A sub-1mA LC SiGe BiCMOS 1.6 GHz Differential VCO with KV Reduction

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Abstract

A 1.6 GHz fully-integrated manufacturable, low-current, low close-in phase noise, differential SiGe HBT BiCMOS voltage controlled oscillator (VCO) is published herein. Low KV with 35 MHz/N nominal has been designed using p-type voltage variable varactors (pVVCs). This VCO was designed and measured in Freescale Semiconductor’s HiP6wRF 0.4 μm SiGe BiCMOS technology for -100 dBc/Hz at 100-kHz frequency offset or -96 dBc/Hz minimum over the entire tuning and trimming range and temperature. The oscillator has a trim/tune range from 1.35 to 1.75 GHz with a 825μAmper core.

1. Introduction

A manufacturable low phase noise voltage controlled oscillator (VCO) is a critical component in modern integrated communication systems. Due to the advancement of integrated resonator technology and lower noise, higher peak fτ active devices, bipolar and Silicon Germanium (SiGe) BiCMOS technology has become one of the most promising and competitive technologies for such manufacturable low-current, low phase noise VCO designs. In addition, higher integration of frequency synthesizer loop filters requires GHz VCOs to implement KV reduction techniques to lower noise pushing sensitivity of the VCO.

VCO publications [1-8] have been presented in recent years displaying the excellent performance of SiGe BiCMOS VCOs. Conversely to RFCMOS VCO designs, SiGe HBT BiCMOS is an optimum choice for manufacturable RF VCOs due to lower flicker noise allowing more loop filter bandwidth selection flexibility, comparable (for even low fτ bipolar) white noise performance for equivalent gms, superior (for higher fτ SiGe HBTs) white noise performance for such high gms, much less active input capacitances due to higher fτ SiGe, lower non-linear harmonic generation than inverter-based designs, more controllable transconductances, and less parasitic sensitivities due to lower current bias requirements than RFCMOS VCOs.

This paper will primarily discuss some design aspects, a test-chip, measurements, and comparison of theoretical, SpectreRF simulation, and measurements of a fully-integrated, low-current, low-KV SiGe VCO for loop filter integration. In addition, higher quality phase noises with bipolar or BiCMOS RF VCOs relative to this VCO will be briefly discussed.

2. LC-VCO Topology Chosen

With much lower flicker noise corners than MOS VCOs, SiGe BiCMOS VCOs provide more flexibility of loop filter bandwidth selection. Further, SiGe LC VCOs are cleaner (lower-harmonic generation) over inverter-based VCOs. With better control of the active transconductance or gm, there are less output current variations over process to refresh resonator losses, and thus less phase noise variations by using SiGe HBTs over RFCMOS. Recognizing that the SiGe HBT is lower white noise for comparable gms to refresh the losses of an equivalent parallel resonator, the SiGe HBT negative gm was also chosen due to superior fτ in a given technology allowing for better noise performance than RFCMOS for less capacitive resonator loading at lower bias currents. Lastly, biased at lower currents, SiGe VCO cores are less sensitive to parasitics providing less sensitivity to parasitic losses in bandwidth and Q reductions… and hence less sensitivity to electromigration problems.

Consequently, the following SiGe HBT VCO topology was chosen for our integrated wireless product.
Since such fundamental RF topologies become very competitive with Q-enhanced resonators and higher ft active devices, the topology consists of an LC resonator with a Cu bump differential 3-port inductor, a 4-bit course tune (a.k.a. trim) network and tuning using cpvc50 varactor devices, SiGe HBTs for negative gm, a near-PTAT core tail current, a capacitive impedance transformer, and SiGe HBT emitter followers with NMOS current mirrors with capacitive gate ac decoupling.

### 3. Design for KV Reduction

Upon integration of a PLL loop filter, die area and manufacturable tolerances become major concerns. Off-chip, the size of capacitors are of no concern. However, on the IC for a given pole frequency, die area must be conserved by designing a loop filter with larger resistances to lessen the amount of capacitance area needed. Thus there is need for a larger loop filter resistance and smaller capacitance on the IC.

The consequence is that a larger thermal noise voltage power associated with a larger resistance is directly coupled to the VCO’s LC tank to modulate the VCO output contributing added phase noise to the spectrum of interest to the PLL and transceiver.

VCO gain (KV) reduction design of the VCO is therefore needed to lessen the contribution of this white noise to the convolution of the VCO phase noise spectrum.

For our design of low KV, Figure 2 shows the SiGe HBT VCO varactor capacitance and derivative of capacitance per tune voltage, or KV, using a pvc50 unit device with number of fingers swept from 3 to 5. A finger size of 3 was chosen for this double-hump low KV design for tuning the center frequency of the design.

### 4. Design for Low Phase Noise & Low Current Consumption

Since our main goal was to design the VCO with the lowest current possible for high volume VCO manufacture within a given phase noise specification ensuring VCO start-up conditions over all manufacturable conditions of process, temperature, and supply variations, figure 3 was generated to determine the inductor size needed for a worst case unloaded quality factor (Q) to ensure a 400 mVP differential output amplitude.

![Fig. 2. Capacitance over tune and the capacitive difference per change in tune voltage for double-hump KV development.]()

For fairly linear GHz VCOs, phase noise was calculated by using Leeson’s equation [9]. The Excess Device Noise Factor was calculated using 2-port LNA theory with the noise components of 3rd order flicker noise, finite Q of the resonator, thermal source impedance, thermal base resistance,
frequency-independent collector shot noise, frequency-dependent DC Beta base shot noise, frequency-dependent AC Beta base shot noise, and tail current noise in the following equation:

\[
P_{\text{noise}}(f, f_{\text{EE}} Q_p) = 10 \log \left( \frac{F T f_{\text{EE}}}{Q_p f_{\text{EE}} (Q_p f_{\text{EE}})} \right)
\]

The convolution of noise sidebands is not modeled here, yet is not as necessary with designs that do not approach the reverse active, triode, or sub-threshold regions. However, such convolutions are much more necessary for inverter-based, harmonic-rich, VCO designs. Thus according to [10], only the 1st coefficient of the impulse-sensitivity function, ISF, is needed and equivalently captured here for SiGe BiCMOS LC VCOs where devices are maintained in their associated near-linear regions over all conditions. As a result, only 1 to 2 maximum sidebands were needed in SpectreRF Pnoise simulations, which will be shown below, to predict the phase noise of this VCO, though 4 sidebands were used for improved accuracy.

5. Inductor Characterization

The differential inductor model was developed by Freescale’s inductor development group for use in this design. The inductor was initially created in Freescale’s CDR1 process technology and converted to HiP6 process technology.

![Fig. 4. Inductor Model.](image)

Figure 5 provides the measured S-Parameters of the inductor via SpectreRF. Note since the S-Parameters were measured in another process, and the inductor was translated to a new process with slightly lighter p-doped substrate with much lower dielectric height, a Q reduction of 10% was assumed. The single-ended (SE) susceptance is nearly –30 mA/V (note a negative susceptance indicating inductive), a SE inductance 3.05 nH, parallel resonant unloaded Q of 23, and conductance of 7.3 mA/V. Though not shown here, these simulations match very well with the inductor model developed from measured data as well.

6. Negative Gm Active Devices

For wireless IC development with rapid design cycle time, SiGe HBTs were also chosen for their superior manufacturable rf performance of low current design ensuring a given phase noise specification. Bipolar devices have very high predictable transconductances and much higher yields over a comparable or advanced RFCMOS topology. In advanced technology nodes, the small additional wafer cost of SiGe is insignificant when considering the additional current consumption, need for additional isolation layers and twin-tub processing, additional flicker noise, possible requirement of additional sub-systems and circuits to compensate for such noise, and yield fallout and cost of test time & packaging for such fallout of such RFCMOS designs.

Figure 6 below is series of single-ended SiGe HBT simulated characterizations at 450 & 900 µAmpere, some over temperature. Note since the single-ended devices were biased at about 400-450 µAmpere each, the 450 µAmpere plots below show, temperature stable bias, that the device ft of 8 – 11 GHz, current gain is 13-17 dB, output-referred noise current is about 13 pA/√Hz, the gm is 1.5-2.2 mA/V, the shunt input capacitance and resistance is about 290 fF and 1.5 – 3k Ω.
8. Other aspects of VCO Design

Further theoretical derivations implemented for design but not covered here include amplitude and noise derivations, startup conditions, low noise negative gm optimization, trim capacitance design for L and C variations and 1 bit overlap for digital trim error allowance, capacitive impedance transformer design, bias circuit design, highly linear, low noise emitter follower design, etc., all over temperature, process, and supply variations.

Figure 7 displays a transient simulation using SpectreVerilog, using Spectre, Verilog, and Verilog-A modules to determine the frequency and trim range of the SiGe HBT VCO while ramping the tune voltage for each digital trim setting. Figure 8 is a close-up view on a curve of Figure 7 above to show the discretized frequency output steps of the Verilog-A module and determination of the nominal KV of the VCO.

9. SiGe HBT VCO TestChip

Needing a very linear output signal for low 2nd harmonic and IIP2, figure 9 shows the custom, high precision layout of the SiGe HBT VCO in Freescale Semiconductor’s HiP6wRF technology. Post fracture total area of the fully-integrated SiGe HBT VCO was 0.49 mm$^2$ including the inductor, all capacitances, and biasing. An integrated open-collector low noise, test buffer design for unity gain was added for measurement.

Recognizing that manufacturable layout techniques are crucial to high volume RFIC development, the RF Designer must be very intimate with, or perform one’s own, RFIC layout. Consequently, very laborious common centroid layout techniques were used in the rf signal path for distribution of process variation among differential signal paths. This and other good design practices clearly improve the IP2 of the linear output signals for a receive system. According to [10], such differential balancing further improves the phase noise performance of the VCO.
10. Measurements of the SiGe HBT VCO

After 1 silicon pass, the tune/trim, KV, & phase noise measurements are shown below. Note since the VCO was implemented rapidly in 8 weeks without back-annotation yet with very methodical layout procedure, measurements indicate the SiGe HBT VCO oscillation frequency was only 50 MHz low when comparing measured to simulated data with assumed parasitics. The cpvvc50 MOS varactors exhibit very linear behavior over their intended ranges. The double-hump KV closely resembles the vvc double-hump capacitance simulated in Figure 2. Phase noise varies from –97 to –101 @ 100kHz offset of fundamental. Note the following measurement data has been taken with a 2:1 balun RF port using the HP4352B VCO/PLL Signal Analyzer with a tune voltage of Vcc/2.

Fig. 10. Measured Trim/Tune Frequency Coverage Range.

Fig. 11. Measured KV over Trim/Tune Coverage Range.

Fig. 12. Measured Phase Noise over Nominal & Trim.

Figure 13 shows the 2nd harmonic is –77.8 dB below the fundamental.

11. Comparison of Theoretical, Simulation, & Measured Phase Noise & Frequency Data

The accuracy and speed of phase noise simulations are always a very fascinating topic often discussed among RFIC design engineers. Consequently, phase noise expectations using Leeson’s Equation and SpectreRF PSS/PNoise simulation has been evaluated below in Figures 14 & 15 relative to the measured data provided. Figure 14 shows theoretical and SpectreRF phase noise matching very well with high trim setting measurement. Note high trim setting refers to all vvc varactors in the off state (actually with about 1/3rd the on capacitance, thus sinking and sourcing about 1/3rd the AC current as in the on state).

Further note when all the trim vvc’s are switched to the trim on state in Figure 15, there is a significant error at close-in offset frequencies of the fundamental. The author believes this error is associated with there being no flicker noise modeling.
of the HiP6wRF vvc’s, which is currently being researched. Since the vvc is essentially a PMOS device without drain-source doping and without a DC current, it indeed should have a flicker noise associated with its AC performance yet is not modeled in the technology. Further Figure 14 shows that when the theoretical corner is moved from 10kHz (as dominated by the SiGe HBTs) to an assumed 900kHz (as dominated by the cpvvc50 devices), the phase noise then closely resembles the measured phase noise of the SiGe HBT VCO at low trim setting. This appears to demonstrate the higher flicker noise corner of RFCMOS technology.

Upon consideration that vvc flicker noise is not modeled in this process, figures 14 and 15 reveal very accurate SpectreRF simulations compared to measured results. Reasons for such simulation accuracy include not only excellent modeling practice within a given technology, a very accurate inductor model and reliance of measured, state-of-the-art custom inductors, varactor, active negative gm, biasing, load and parasitic modeling. Since bias circuits and supply references can generate a large amount of noise, exclusion of these circuits from phase noise simulations have provided optimistic phase noises of as much as 6-8 dB in formerly studied RF VCOs. However, all buffer, VCO bias, & buffer bias circuits have been included in these simulations.

Additionally beyond good modeling, this simulation accuracy can be attributed to use of SpectreRF PSS/Pnoise in VCO design. According to SpectreRF PSS/Pnoise simulation theory in [10], unlike conventional analysis, SpectreRF “computes frequency conversion effects”.

With periodic systems, there are 2 effects that act to translate noise in frequency.

1. For noise sources, such as shot noise that are bias dependent, the time-varying operating point acts to modulate the noise sources (i.e. big swings in these LC oscillators to create large fundamentals for lower dBC).

2. The transfer function from the noise source to the output is also periodically time-varying and therefore acts to modulate the contribution of the noise source to the output.

Modulation (thus) yields a multiplicative effect in the time domain, and therefore in the frequency domain, the spectrum of the noise source is convolved with the spectrum of the transfer function. The transfer function is periodic and thereby has a discrete line spectrum.

Convolution with a discrete spectrum involves a countable number of scale, translate, and sum operations. The final result of the analysis is the sum of the noise contributions both up-converted and down-converted to the desired output frequency. Consequently, the ‘time-varying’ linear system of an oscillator describing the small-signal response v(t) is multiplied by an operator L(t) which has poles at the harmonics of the oscillation frequency, "numerical calculations of the noise at nearby frequencies become inaccurate if treated in a naive manner." This also gives additional insight of the importance of selecting linear topologies and emphasizing good DC bias design for improved phase noise designs.

12. Bipolar/BiCMOS VCOs and higher quality phase noises.

Upon consideration of such a bipolar VCO obtaining high-quality phase noise, Figure 16 shows, using the technology-dependent theoretical model used in the previous 2 figures, how such a bipolar or BiCMOS VCO can indeed achieve high quality phase noise, provided proper biasing conditions are considered for each condition. The phase noise plot of Figure 15 has been implemented at 100 kHz offset of 1.6 GHz fundamental. Assuming the supply is large enough to handle such signals and take full advantage of the large breakdown
voltage of the bipolar device, figure 17 further shows the differential amplitude generated to achieve such phase noise from Figure 16. Approximately 3.4 Vp, or 6.8 Vpp, differential (or 1.7 Vp single-ended) voltage swing would be required which is possible for a 2.7 volt supply with margin.

Generating a LO frequency with 4-bit trim to compensate for resonant L & C variations, the SiGe HBT VCO possesses a total measured frequency range of approximately 1340-1725 MHz, while the unbackannotated simulated frequency trim and tune range of 1.375-1.775 GHz. At nominal temperature and a supply of 2.65 V, this SiGe HBT VCO lot has overlapping frequency coverage, a desirably low KV (~15-60 MHz/V), good phase noise which has not violated a –92 dBc @ 100kHz offset specification, very low 2nd harmonic level, and very low DC current. Lastly, low current modern bipolar and BiCMOS technologies can easily compete and exceed RFCMOS fully-integrated VCO performances.

TABLE I
THE 1.6 GHz SiGe HBT VCO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
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<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.65 – 2.75</td>
<td>V</td>
</tr>
<tr>
<td>Oscillator core current</td>
<td>825</td>
<td>µA</td>
</tr>
<tr>
<td>Tuning range @ 1.57 GHz</td>
<td>±12.7</td>
<td>%</td>
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<tr>
<td>Phase Noise @ 100 kHz</td>
<td>-97</td>
<td>dBc worst case</td>
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<tr>
<td>KV</td>
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<td>MHz/V</td>
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<td>VCO area</td>
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</tr>
</tbody>
</table>

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14. REFERENCES


