A Low-Power Dual-Band BiCMOS Front-End for Wireless LAN Receivers

Corrado Carta, Rolf Vogt and Werner Bächtold
Electromagnetic Fields and Microwave Electronics Laboratory (IFH),
Swiss Federal Institute of Technology (ETH), 8092 Zurich, Switzerland
email: carta@ifh.ee.ethz.ch

Abstract

This paper presents a dual-band RF front-end for WLAN low-IF receivers, operating in the 2.4 GHz ISM band and the three 5 GHz U-NII bands. The RF receiver uses an LNA with dual input stages, replacing the use of multiple independent LNAs operating at different bands, and one multi-band image rejecting mixer, which exploits the inherent broadband frequency response of multi-stage polyphase filters and singly-balanced active mixers. The chosen architecture avoids the use of switches in the RF path by means of a dual-band resonator at the LNA-mixer interface. Fabricated in a 0.25 µm 47 GHz-f_t BiCMOS technology, the circuit exhibits 33.4 dB of conversion gain, 4.1 dB of NF and -16.6 dBm of iIP_3 in the 2 GHz mode, while in the 5 GHz mode conversion gain is 27 dB, NF is 8.6 dB and iIP_3 is -11.6 dBm. Power consumption is 14.9 mW for the low-frequency mode, and 18.7 mW for the high-frequency mode. Making use of no external components, this chip provides a good basis for the realization of low-cost receivers for dual-band operation.

1. Introduction

The 2.45 GHz industrial scientific medical (ISM) band is presently the most used for wireless LAN applications. The desirable migration to the 5-6 GHz unlicensed-national-information-infrastructure (U-NII) bands, which can make possible higher data rates, must necessarily go through coexistence, making multi-band devices more attractive. These demands are often addressed by integrating several independent sets of RF front-ends [6, 8]. However, some of the blocks needed are inherently broadband and this feature can be exploited to reduce the overall number of components, dice area and cost [5, 7].
This paper presents the low-power implementation of an architecture which allows making use of the broadband frequency response of singly-balanced active mixers and multi-stage polyphase filters in low-IF multi-band receivers.

Fig. 1 shows the block diagram of the receiver. It consists of a dual-input LNA and an image-rejecting mixer, which is in turn constituted of a pair of matched mixers and two polyphase filters. The LNA has two inputs: the one in use must be selected with an external control voltage. The amplified signal is fed through a switchless connection to the mixer pair and downconverted to a 40 MHz IF. The LO polyphase filter generates quadrature signals needed for both input bands, while image rejection over the 30-50 MHz band is provided by the IF polyphase filter.

2. Circuit Design

Fig. 2 shows the schematic of the HBT cascode dual-band LNA. The emitter current of T_3 flows completely in T_1 or T_2, according to the selection of a control voltage V_{mode}, which sets the position of a bias switch. When active, the two inputs are power and noise matched to a 50 Ω source.
The collector load of T_3 is designed to provide, together with the mixer input capacities, a high impedance at both input bands, thus allowing a switchless connec-

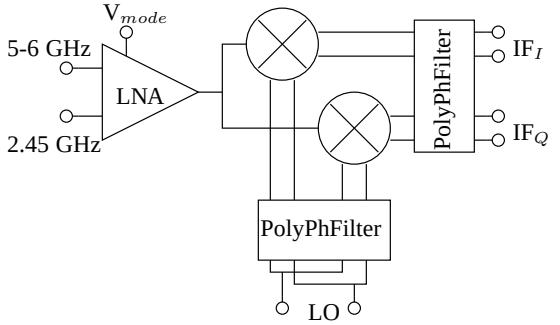

Figure 1. Block diagram of the dual-band RF front-end.

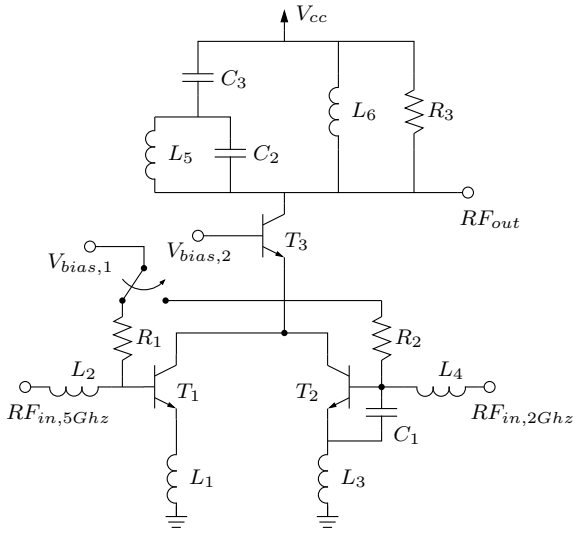

Figure 2. Schematic of the dual-band LNA.

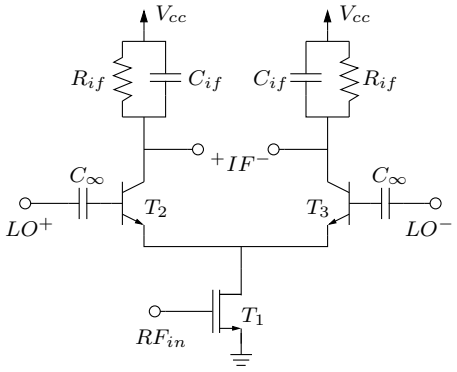

Figure 3. Minimal-embodiment schematic of the singly-balanced mixer.

tion to the following stage. The shunt resistor R_3 lowers the resonator quality factor to fulfill the bandwidth specifications. The LNA was designed to provide 20 dB and 18 dB of voltage gain for the 2 GHz and 5 GHz band respectively, with 1.6 dB and 2.1 dB noise figures, for current consumptions of 2.2 mA and 3.9 mA from a 2.4 V power supply.

Fig. 3 shows the schematic chosen for both of the matched BiCMOS active singly-balanced mixers [4]. The RF transconductance is implemented with a non-degenerated common source nFET, whose input capacity resonates with the LNA load in the two operating bands, in order to offer a high impedance to the preamplifier. The mixer core is an HBT differential pair driven by the differential LO voltage; the LO port is not matched to any particular frequency, allowing the exploited broadband operating range. The IF load is a resistor in parallel with a capacitor: while the resistor R_{if} sets the conversion gain, the capacitor C_{if} reduces the IF output bandwidth, thus rejecting the LO feed-through. Each mixer was designed to provide 16 dB of voltage conversion gain with a current consumption of 2 mA from the 2.4 V power supply.

The LO polyphase filter is the cascade of three passive RC stages [1]. In order to provide amplitude balance and phase quadrature for both the operation modes, the first stage has its cut-off frequency in the 2 GHz band, while the last two in the 5 GHz one: the frequency response of the series of the three stages can offer sufficient amplitude and phase balance in both the operating bands. The IF polyphase filter is the cascade of two stages, in order to achieve IRR over the 20 MHz bandwidth required for the main WLAN standards.

3. Experimental Results

3.1. Fabrication

The circuit was fabricated with the commercial IBM BiCMOS 6HP process [3]. At optimum bias current, the HBTs yield transit frequencies f_t up to 47 GHz and minimum noise figures NF_{min} of around 1.2 dB at 5 GHz. The process is targeted for RF, analog and mixed signal applications, having a 4 µm thick Analog Metal and a maximum dielectric stack of 10.1 µm for low-loss interconnect. This, together with the deep-trench insulations and patterned poly-silicon shields, allows the implementation of inductors with quality factors up to 19 at 5 GHz.

A photograph of the circuit, implemented on a 0.73 mm^2 active area, is shown in Fig. 4. Total area measures 1.79 mm$\times$1.29 mm.

3.2. Measurements

Fig. 5 shows the measured frequency behavior of conversion gain, image-rejection ratio and iIP_3: the circuit is operated in low-frequency mode for frequencies up to 3.4 GHz, in high-frequency mode otherwise. Both conversion gain and IRR show dual-band response: the two conversion gain peaks are due to the double resonance of the LNA load, while IRR values are the result of the quadrature LO signals generated on chip by the LO polyphase filter.

Fig. 6 shows the frequency behavior of the input matching for the two input ports in the corresponding operating mode.

Fig. 7 and Fig. 8 show in greater detail the measurement re-

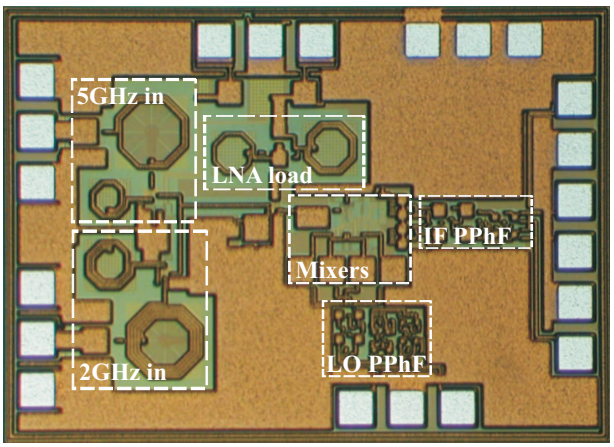

Figure 4. Chip microphotograph of the double-band image-reject receiver. Area shown measures 1.79 mm×1.29 mm.

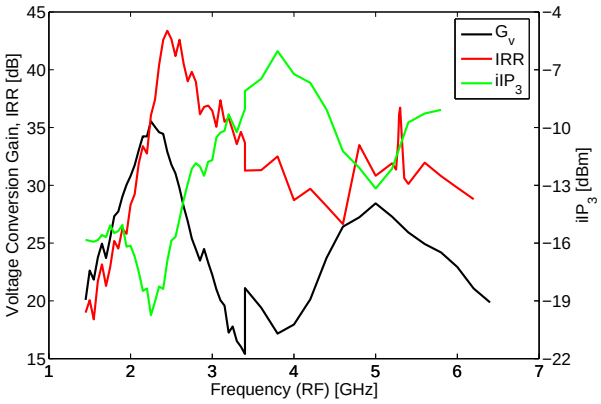

Figure 5. Conversion gain, image rejection ratio and iIP_3 of the receiver. The circuit is operated in mode "low" below 3.4 GHz and mode "high" above that. LO power levels are 0.8 dBm and 2.4 dBm respectivley.

Table 1. Summary of measured results

RF band	[GHz]	2.45	5.2	5.3	5.775
Conv. Gain	[dB]	33.4	27.0	26.5	24.5
IRR	[dB]	43.3	31.9	36.7	30.8
NF	[dB]	4.1	8.6	8.6	10.1
$P_{1\ dB}$	[dBm]	-26.0	-19.0	-19.3	-16.7
iIP_3	[dBm]	-16.6	-11.6	-11.0	-9.3
S_{11}	[dB]	<-17.5	<-18.0	<-16.0	<-18.0
LO	[dBm]	0.8	2.5	2.4	2.4
LO to RF	[dB]	62.8	63.5	67.4	54.4

sults for the 2.45 GHz band: in Fig. 7 NF, signal and image conversion gain, in Fig. 8 $P_{1\ dB}$ and iIP_3 extrapolation. Table 1 summarizes the measured performances of the prototype over the 2 GHz ISM band and the three 5 GHz U-NII bands. Power consumption is 14.9 mW for the low frequency mode and 18.7 mW for the high frequency mode.

Performances are satisfactory in the 2 GHz mode, but suffer of some degradation of NF in the 5 GHz mode. This is partly due to inaccuracy in LNA double-band load modelling, which peaks at 5 GHz instead of 5.5 GHz as simulated, and test-board inductive parasitics on the ground connections, which are more critical in the high-frequency operation.

The IRR measurements in the high-frequency range are probably affected by test board parasitics as well. These result in unwanted coupling and worsen the observed results. The values shown in Fig. 5 and Table 1 can be considered as worst-case estimations.

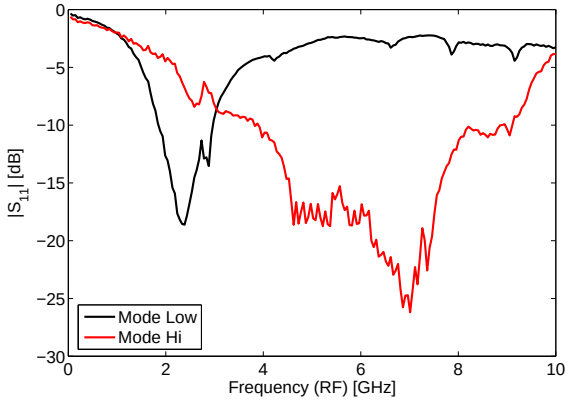

Figure 6. Input matching of the two ports.

4. Conclusions

The design and implementation in a 47 GHz-f_t BiCMOS technology of a low-power dual-band RF front-end has been presented. The circuit shows multi-band functionalities, confirming the validity of the chosen architecture. The measured performances are close to meet the specifications for the RF front-end of receivers compliant with IEEE WLAN standards at 2 GHz [9] and 5 GHz [2]. Making use of no external components and very low DC power, this chip provides a good basis for the realization of WLAN low-cost receivers for dual-band operation.

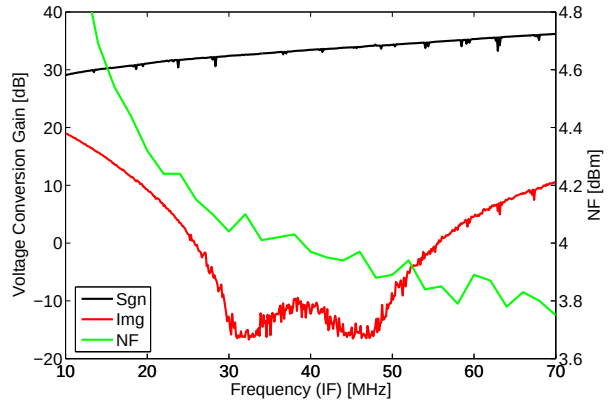

Figure 7. Voltage conversion gain and NF for the 2 GHz band.

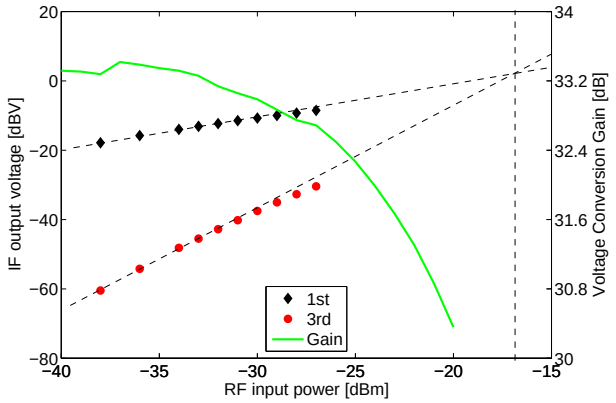

Figure 8. iIP_3 and $P_{1\ dB}$ in the 2 GHz band.

5. Acknowledgment

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