Performance of a 12GHz Monolithic Microwave Distributed Oscillator in 1.2V 0.18µm CMOS with a New Simple Design Technique for Frequency Changing

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Abstract

A monolithic distributed oscillator (DO) is designed and fabricated using an n-FET-based Traveling Wave Amplifier (TWA), coplanar waveguides (CPW) and a proposed coplanar bend structure called a 'folded CPW'. The measured loss S_{21} (dB) of the 'folded CPW' is 1.259dB at 10GHz before pad de-embedding. Experimental measurements are reported for the first time for a DO using an industry-standard 0.18µm CMOS technology, (with a bias of 1.8V). The oscillator operates at 12.0GHz with 5.77dbm and the measured phase noise is –115.16dBc/Hz at 1MHz offset. The signal power in the harmonics is very low, -34dBm in the 2nd harmonic. The frequency of oscillation can be increased for this oscillator by 170MHz by varying the dc bias. Finally, a technique to change the frequency by varying the inter-cell inductive loads is proposed.

1. Introduction

Two monolithic Distributed Oscillators (DOs) using TWA with low-loss CPWs as inductive elements are reported. A TWA is converted to a DO by introducing a feedback loop, i.e. a 180-degree bend in the CPW. Traditional non-TWA oscillators use relatively complicated circuits with large area on-chip inductors and capacitors. Our TWA-based designs use only n-FET transistors, CPWs and a feedback loop. We first propose a coplanar structure which balances the parasitic inductance and capacitance of the feedback loop, called a 'folded CPW'. The use of only n-FETs and FET loaded coplanar waveguides matched to 50Ω impedance results in fast rise and fall times [1], and a high oscillation frequency of 12GHz is achieved.

According to [2], in a loss-less idealized approximation given unity loop gain, a distributed oscillator can oscillate at frequency $f_T\pi/2$. In our 0.18 micron CMOS process, f_T can reach 50GHz and the ideal frequency can reach 78GHz. This analysis shows the potential high frequency operation of DOs in 0.18µm CMOS, even with real-life losses. Our first oscillator design, hereafter called OSC-1, is based on the TWA of [3] and is similar to that reported in [1]. It uses five 60µm width single n-FET cells and CPWs (rather than CPS as in [1]). OSC-1 exhibits a measured fundamental frequency of 12.0 GHz with 5.77dBm signal power level and –115.16dBc/Hz phase noise at 1 MHz offset. Simulations of OSC-1 were reported in [4] without a capacitor in the feedback path (frequency 14.75GHz, -2.5dBm, phase noise -110dBc/Hz at 1MHz offset and power in 2nd harmonic is -30dBm). Further simulations are reported for OSC-1 indicating VCO operation, after incorporating a capacitor in the feedback path (see Fig. 1) to overcome the drop in amplitude as the bias is varied (as used in [5]).

A second DO is also proposed, an optimized four stage design using 2-transistor gain cells, similar to the 5-stage TWA design we reported in [4]. This design will be referred to as OSC-2. The n-FET cascode gain cell [6] consists of a common source stage with a common gate stage [4], [6]. Comparing the 5-stage design of OSC-1 and OSC-2, OSC-2 has a higher output level, likely due to the use of the cascode gain cells.

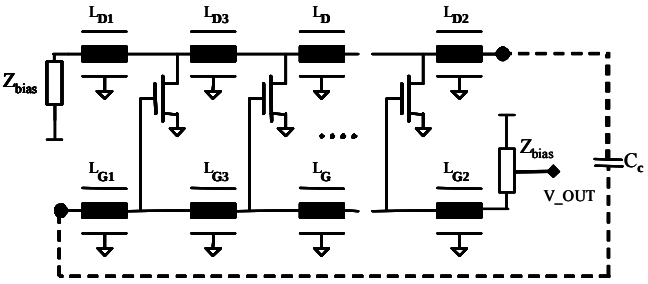

Figure 1. Schematic of the DO with coupling capacitor C_c incorporated in simulation after measurements.

Finally, we propose a new simple design technique to vary the oscillation frequency over a wide range by varying the inductive values of the CPWs between gain cells. Previous TWAs have used inductive elements with a fixed value of L between gain stages and L/2 at the start and end-ports, a trend which has been valid for 20 years in distributed solid state circuit design.

2. Design of the distributed oscillator and coplanar structure

A TWA-based oscillator is designed in ADS by adding a feedback loop, as illustrated in Figure 1. Conceptually,

instead of using a single large (i.e. 'lumped') n-FET transistor, this transistor can conceptually be divided into five equal segments [1]. The five gate inputs are connected with CPWs of impedance Z_{line} as are the five drain outputs, where Z_{line} is given by

$$Z_{line} = \sqrt{\frac{L_{line}}{C_{line}}}$$

where L_{line} and C_{line} are the inductance and the capacitance per unit length of the coplanar waveguide.

The sum of transistor widths is therefore the same as the lumped FET. The parasitic capacitance of each transistor C_{FET}, which loads the CPW, is only one fifth of the lumped FET. The characteristic impedance Z_{line} of coplanar transmission lines is selected as higher [1] than the desired input and output impedances Z (=Z_0) of the DO, since the parallel FET capacitance is added to C_{line}.

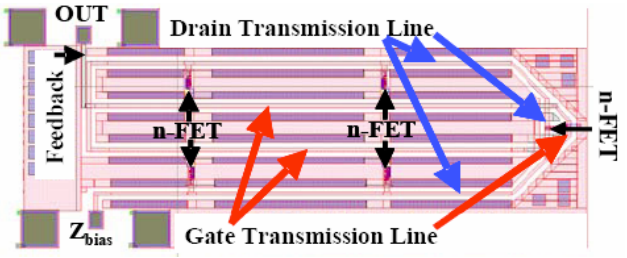

Figure 2. Layout of the monolithic microwave distributed oscillator (top view) in 0.18µm CMOS with G-S-G pads for measurements, chip area: 1.5x0.65 sq. mm.

Ideally, the feedback connection should have zero loss and zero delay [1], which can be approximated by folding the gate and drain transmission lines in a U-shape as used in [1]. The inner U transmission line is used for the gate line, while the outer U line is used for the drain line, as shown in Figure 2. This layout brings the output of the drain line close to the input of the gate line, but introduces signal paths of different length [1]. To keep the drain and gate line lengths equal, we introduce an inversion where the drain coplanar signal line assumes the inner path as shown in Figure 3, a different approach from [1]. We call this design structure made for path length equalization the "folded CPW", as shown Figure 3.

3. Measurements of coplanar structure and oscillator OSC-1

The 'folded CPW' of Fig. 3 was fabricated and measured with a probing system and vector network analyzer using S-G (signal-ground) probes for signal-ground pads, rather than the G-S-G probes used for measurements as in [3], [4]. The measured loss S_{21} (dB) versus frequency of the "folded CPW" of Figure 3 is shown in Figure 4 before pad de-embedding, with 1.259dB loss at 10GHz. The measured input and output reflections before pad de-embedding are S_{11}= -24.6dB and S_{22}= -24dB at 12GHz.

The measurements were de-embedded for the pads using previously measured s-parameter data of ground-signal-ground pads [3], which should be accurate as the pads have similar size and the substrate is similarly grounded. The folded CPW exhibits 0.8dB loss at 10GHz after pad de-embedding. For our previously characterized straight line CPWs reported in [3], [4], the measured loss was 0.64dB/mm at 10GHz. Our straight-line CPW would have a loss of only 0.67 dB/mm at 10GHz [3], [4]. By adopting two 45-degree bends in the folded CPW, the added loss is only 0.13 dB. From the loss point of view, two 45 degree bends are preferable to two arbitrary angle bends such as 30 or 60 degrees, which yield higher reflection losses. Furthermore, non-standard bends may create design rule violations.

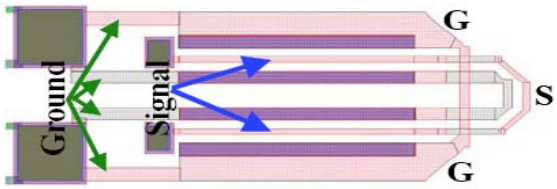

Figure 3. Layout of the coplanar test structure 'folded CPW' (top view) used in the bend path of the gate line.

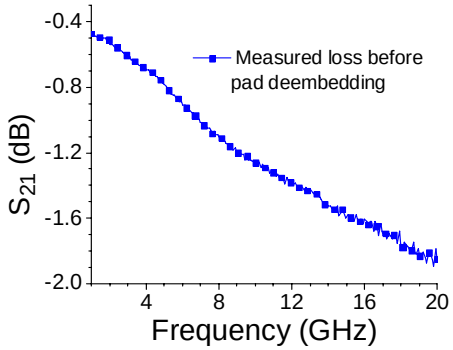

Figure 4. Measured loss S_{21} (dB) versus frequency of the coplanar test structure of Figure 3.

OSC-1 was measured with a probing station and two spectrum analyzers, one of which is capable of phase noise measurements using a built-in software module. The measured power for the OSC-1 is shown in Figure 5. A marker shows the fundamental is at 12.00GHz with a power of +5.77dBm, and the 2nd harmonic is at 23.92GHz with a power of -34dBm. OSC-1 operates at a bias of 1.8V and 60mA. By changing the bias to 1.2V, the performance was shifted up to 12.17GHz with -8dBm output power.

The measured phase noise spectrum of OSC-1 is shown in Figure 6. A 10 dB coupler was used to reduce high signal power from reaching the measuring spectrum analyzer and producing any nonlinearity, as done in [1] using a 6dB coupler. The measured phase noise is -

115.16dBc/Hz at 1 MHz offset from the 12GHz carrier in OSC-1. The power and phase noise figures for OSC-1

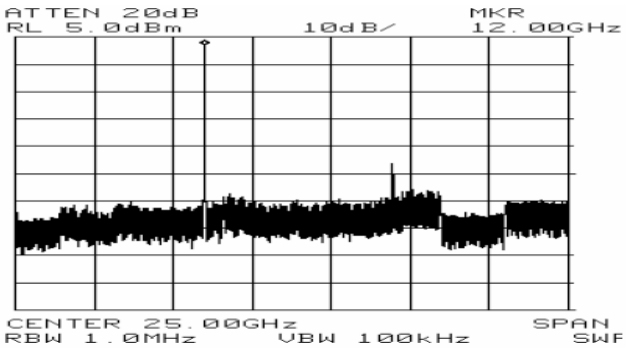

Figure 5. Measured power spectrum of the Osc-1 with marker showing that the fundamental is at 12.00GHz, +5.77dBm (includes 2.6dB loss from the testing systems).

implemented in industry-standard silicon CMOS are compared to prior reported results (implemented with non-standard CMOS [1] and BiCMOS [5] processes) in Table 1 and Figure 7 respectively. OSC-1 offers the best power and phase noise results of DOs in the literature.

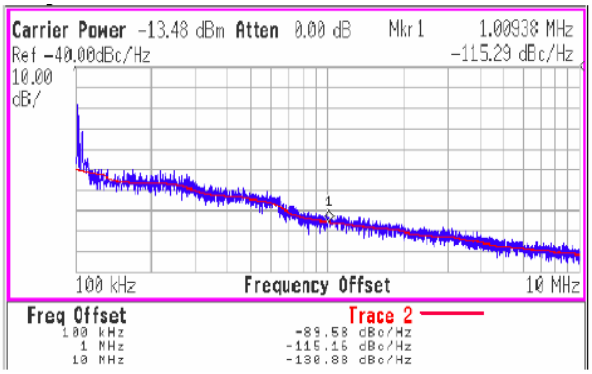

Fig. 6. Measured phase noise spectrum of the Osc-1. It is -115.16dBc/Hz at 1 MHz offset from the carrier.

The carrier-to-noise ratio (CNR) has been calculated according to [7], where CNR= (negative phase noise) in dBc/Hz. The CNR is normalized with respect to fundamental frequency of operation and power consumption, to yield CNR_{norm} as in [7]. The CNR_{norm} can be used as a "Figure of Merit" (FoM) [7]. For OSC-1 the CNR_{norm}= FoM = 176.41dBc/Hz.

4. VCO-Like operation

A simple modification of the DO in Figure 1 is proposed to achieve VCO-like operation, i.e., the introduction of a capacitor in the feedback path (the dashed line in Figure 1) for ac coupling, similar to [5]. The circuit was simulated in the ADS Harmonic Balance simulator. The coupling capacitor allows for the independent control of the dc voltage in the gate and drain lines. By using single n-FET gain cells with a width of 30µm, the oscillator simulation reports a fundamental at 17.921GHz with 5.1dBm output power level (much higher than [4]) , at a drain bias of 1.8V and a gate voltage of 1.2V. The higher

Table 1

Frequency (GHz)	Power level (dBm)	Operating Voltage,V	Reference
16.8	-3.5	1.3	[1]
12.0	-15.37	2.5	[5]
10	-4.5	2.5	[5]
12	+5.77	1.8	This work

frequency (17.92 GHz versus 12 GHz in OSC-1) is due to the smaller width of the n-FETs. By increasing the drain voltage by 0.2V while keeping the gate voltage constant at 1.2V, the frequency is increased by 60MHz, with a 1

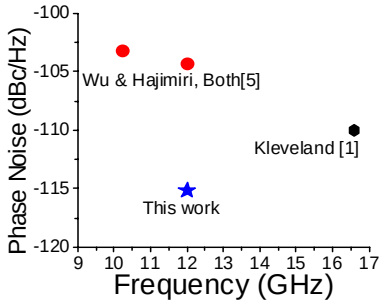

Figure 7. Comparison of measured phase noises for DOs.

dBm increase in output level. By decreasing the gate voltage by 0.2V while keeping the drain voltage constant at 1.8V, the frequency is increased by 60MHz with a 1.3dBm decrease in output. We observe that this design variation results in a high frequency VCO with large amplitude, achieved by tuning the parasitic gate and drain capacitances ("inherent varactors" [5]) of the n-FETs.

5. Simulation of Oscillator-2

OSC-2 shown in Figure 8 is based on similar five stage DO reported in [4], and uses 50µm wide n-FET transistor. The gain cell is an n-FET cascode formed by a common

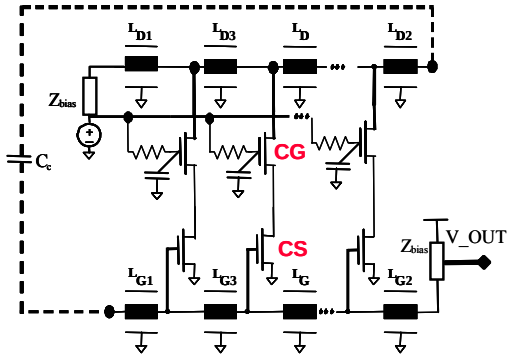

Figure 8. DO with n-FET cascode gain cells.

source stage with a common gate stage, as in [4], [6]. The

detailed schematic is shown in Figure 8, with a capacitor in feedback path. Simulation at V_{DD}=1.8V and V_{GG}=1.2V indicates a fundamental of 12.67GHz with 1.5V peak amplitude (figure 9) with 45mA peak current.

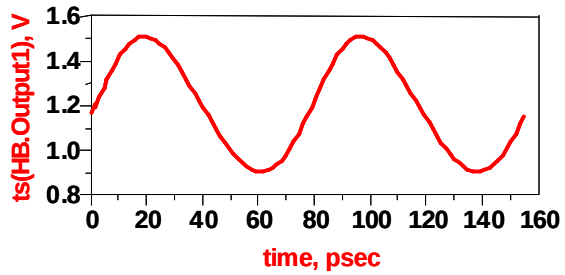

Figure 9. Time domain waveform of OSC-2.

5. Static Frequency Changing

The impedance of the CPWs between the gain cells can be changed, to yield different static oscillation frequencies. The inductances L_{D1}, L_{G1} and L_{D2}, L_{G2} were varied from L/2 up to 3L/2 in steps of L/2. The simulated results are reported in the Table 2 for OSC-1 and OSC-2 (parameters not listed have values of L/2). The simulations are also reported for L_{D3} and L_{G3} situated between the first two gain cells, shown in Figures 1 and 8. Table 2 shows that OSC-2 achieves a 2.12GHz frequency variation (12.63 GHz – 10.55GHz) by changing one or two L values. OSC-1 achieves a frequency variation of 2.291GHz. The simulated frequencies are acknowledged to be optimistic, but we expect the manufactured designs to exhibit similar trends and variations.

6. Conclusion

A monolithic distributed oscillator (OSC-1) has been designed and fabricated using an n-FET based TWA, coplanar waveguides (CPW) and a proposed coplanar structure called 'folded CPW' in industry standard 0.18 micron CMOS technology. The oscillator uses uniform 60 micron wide transistors, and operates at 12.0GHz with 5.77 dBm power level, with a phase noise of –115.16dBc/Hz at 1 MHz offset. We observe that the frequency can be increased by 170MHz by varying the dc bias. This observation leads to a proposed variation of OSC-1 with VCO operation, wherein a bypass capacitor is added. Simulated results have been reported. A second four stage distributed oscillator is also proposed, where each gain cell uses an n-FET cascode (similar to a 5-stage circuit reported in [4]). According to the ADS HB simulator, this distributed oscillator oscillates at 12.67GHz with -1.5dBm power.

Table 2

Changed Values of Inductive CPWs from: $L_{D1}=L_{G1}=L_{D2}=L_{G2}=L/2$ $L_{D3}=L_{G3}=L$	OSC-2 Freq: (GHz) 12.67	OSC-1 Freq: (GHz) 17.921
$L_{D1}=3L/2$	12.05	17.71
$L_{D1}=L$	12.35	17.76
$L_{G1}=3L/2$	11.0	15.87
$L_{G1}=L$	11.75	16.83
$L_{D1}=L_{G1}=3L/2$	10.55	15.74
$L_{D1}=L_{G1}=L$	11.75	16.70
$L_{D2}=3L/2$	11.0	15.87
$L_{D2}=L$	11.75	16.83
$L_{G2}=3L/2$	12.63	17.88
$L_{G2}=L$	12.42	17.54
$L_{D2}=L_{G2}=3L/2$	11.0	15.63
$L_{D2}=L_{G2}=L$	11.75	16.75
$L_{D3}=3L/2$	12.50	17.69
$L_{D3}=2L$	12.13	17.51
$L_{G3}=3L/2$	12.45	16.91
$L_{G3}=2L$	12.07	16.63
$L_{D3}=L_{G3}=3L/2$	12.11	17.0
$L_{D3}=L_{G3}=2L$	11.72	16.28

7. Reference

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