A Low Power CMOS Distributed Amplifier

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***Abstract*— A CMOS distributed amplifier (DA) intended for ultra-wideband (UWB) wireless applications is presented. The proposed distributed amplifier employs current reuse technique to achieve low power consumption. This work is implemented in 0.18-μm CMOS technology and shows a 8GHz bandwidth. The amplifier provides a maximum forward gain (S_{21}) of 5.2 dB while drawing 23 mW from a 1.8-V supply. A noise figure as low as 4.7 dB and an P-1dB of 4 dBm have been demonstrated.**

I. Introduction

The distributed amplification using a cascade of discrete transistors is a technique wherein a more relaxed gain-bandwidth trade-off is obtained than a conventional amplifier. By combining the input and output capacitances of the transistors with lumped inductors to form artificial transmission lines, DA is capable of giving a flat, low-pass response up to very high frequencies. Consequently, DAs find many applications in wideband systems such as UWB which has lately drawn an enormous attention and interest due to its potential for short-range high-speed wireless applications including automotive collision-detection systems, through-wall imaging systems, high-speed indoor networking, etc..

GaAs based DAs were well developed in 1980's [1]-[4], owing to high transistor cut-off frequencies, low loss and high isolation of the III-V substrate. Recently, DAs in complementary metal oxide semiconductor (CMOS) process have emerged due to their integration ability with baseband circuits, the enhancement of the cut-off frequency of silicon transistors, and low cost [5]-[10].

Although, the wideband characteristic of DAs is suitable for UWB systems, the total power consumption of all cascaded stages of DAs tends to be too high to meet the low power requirement which is one of the most important design criteria in the applications for UWB systems [11]. The motivation of this paper is to design a CMOS DA with power saving topology. In this paper, we design and analysis a low power CMOS DA employing current reuse technique. Measurement results suggest this work consumes the lowest power among previously reported DAs.

II. Amplifier Analysis

A. CMOS Distributed Amplifiers

A schematic of the conventional CMOS DA is shown in Fig. 1. The common source based DA has a cascade of N identical NMOSs with their gates connected to a transmission line with characteristic impedance of Z_g and spacing of l_g, and their drains connected to a transmission line with characteristic impedance of Z_d and spacing of l_d, respectively. The shunt capacitances of each amplification stage are isolated from one another, as a result, the total gain can be increased by cascading more amplification stages with no bandwidth degradation at the same time. For matched input and output ports, the power conversion gain of common source based DA can be obtained by using the transmission line theory.

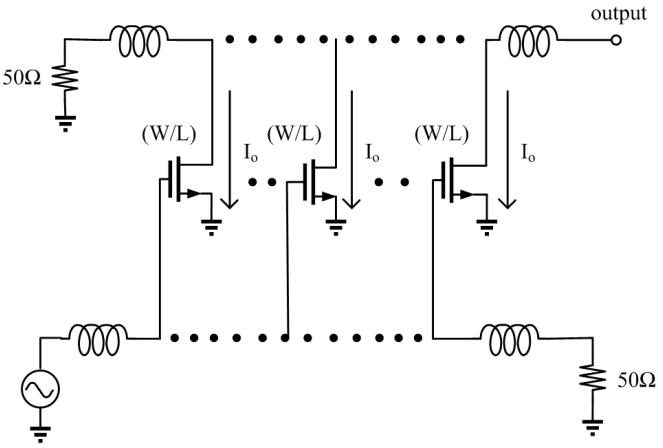

Fig. 1. The schematic of a common source based DA.

$$G = \left| \frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}} \right|^2 \frac{Z_d Z_g}{4} g_m^2, \qquad (1)$$

where γ_g and γ_d are the propagation constants of the gate and drain paths [12]. For a DA which has a cascade of certain amplification stage number N and fixed transmission line conditions, equation (1) shows that the power conversion gain of a DA is proportional to the square of device's transconductance value, which is defined to be g_{m0} herein for a NMOS with length of L_o and width of W_o. The DA's gain is further simplified to be

$$Gain_o = K_o g_{m_o}^2 = K_o \times 2\mu_n C_{ox}(W_o/L_o)I_o, \qquad (2)$$

K_o is defined to be a device irrelevant parameter.

To reduce the power budget, the current reuse technique [13] is employed in proposed DA.

B. Current Reuse Technique

As shown in Fig. 2, a PMOS and a NMOS with inverter configuration are together the base transconductance amplifier stage in proposed DA. The goal is to achieve the gain-bandwidth product with less current. In order to get the same

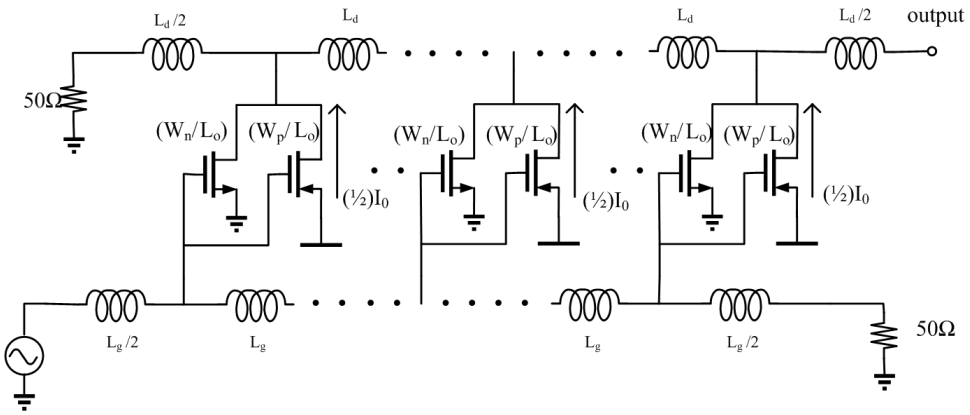

Fig. 2. The schematic of the proposed DA.

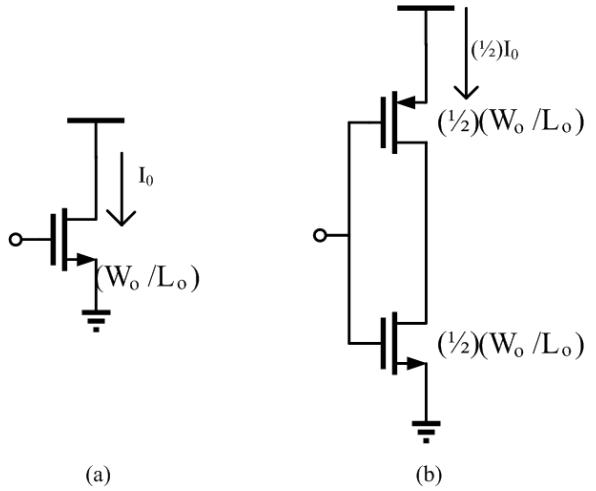

Fig. 3. Comparison of current consumption between the conventional DA (a) and proposed DA (b).

bandwidth as that of a common source based DA, the total device width of PMOS and NMOS of proposed DA is selected to equal the device width of the common source based DA. Accordingly, the device dimensions of PMOS and NMOS in proposed topology are therefore

$$\frac{W_n}{L_o} = \frac{W_p}{L_o} = \frac{1}{2}\left(\frac{W_o}{L_o}\right). \tag{3}$$

Consequently, the bandwidth of presented current reuse DA is nearly the same as that of the basic common source configured counterpart. As shown in Fig. 3, the input capacitance of current reuse topology is equivalent to the input capacitance of common source topology, while only half of the current is consumed.

C. Gain-Bandwidth Product

The transconductance of each amplification stage consisting of a PMOS with device dimension of W_p/L_o and a NMOS with device dimension of W_n/L_o in inverter configuration is

$$g_{mt} = g_{mn} + g_{mp} = \frac{1}{2}g_{mo} + \sqrt{\frac{\mu_p}{\mu_n}}\frac{1}{2}g_{mo}. \tag{4}$$

From equation (2) and (4), the gain of proposed current reuse DA is thus

$$\begin{aligned} Gain' &= K_o(\frac{1}{2}g_{mo} + \sqrt{\frac{\mu_p}{\mu_n}}\frac{1}{2}g_{mo})^2 \\ &= \frac{1}{4}(1+\sqrt{\frac{\mu_p}{\mu_n}})^2 Gain_o. \end{aligned} \tag{5}$$

The gain-bandwidth product per unit power of common source DA is presented as FOM_o for performance evaluation.

$$FOM_o = \frac{G_o \cdot BW_o}{P_o}. \tag{6}$$

Since the proposed DA has power consumption of $P_o/2$, gain of $(\sqrt{\mu_n}+\sqrt{\mu_p})^2 G_o/4\mu_n$, bandwidth of BW_o, the gain-bandwidth product per unit power of proposed current reuse DA is thus

$$\begin{aligned} FOM' &= \frac{(\sqrt{\mu_n}+\sqrt{\mu_p})^2 G_o/4\mu_n \cdot BW_o}{P_o/2} \\ &= \frac{(\sqrt{\mu_n}+\sqrt{\mu_p})^2}{2\mu_n} FOM_o. \end{aligned} \tag{7}$$

If $\mu_n \approx 3\mu_p$, then $FOM' \approx 1.25 FOM_o$. That is, the performance of proposed current reuse DA is 25 percent enhanced than the conventional common source topology in today's mainstream CMOS technology.

III. Design Example

Based on aboved design concepts, a low power current reuse distributed amplifier was implemented in the United Microelectronics Corporation (UMC) 0.18-μm 1.8-V RF CMOS process. Since the input voltage on the gate line of DAs decays exponentially, the gain of a cascade of N amplifier stages will not always increase as the increase of cascade stage number N. In contrast, there will be optimum value of cascaded stage number N_{opt} that maximizes the gain of a DA [12]. Three inverter amplification stages were designed with PMOS and NMOS gate width of 150μm to achieve 8-dB gain after analyzing N_{opt} and attenuation of gate and drain lines. The chip photograph is shown in Fig. 4. The chip size of the DA core is 0.7×1.2 mm^2. The characteristic impedance Z_g and

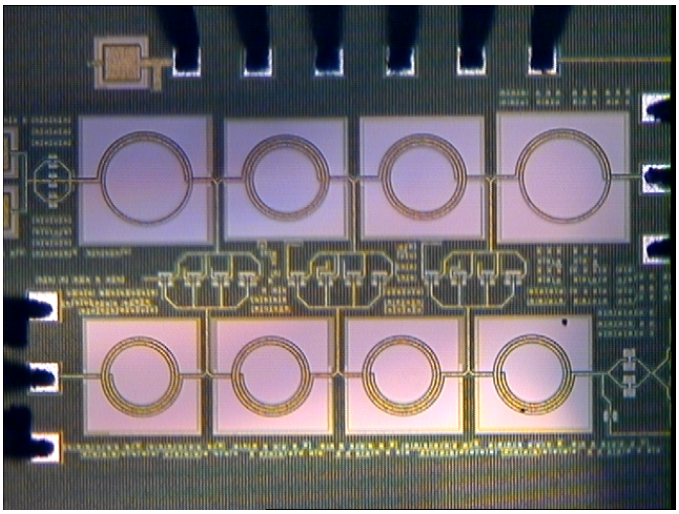

Fig. 4. Microphotograph of the low power CMOS DA.

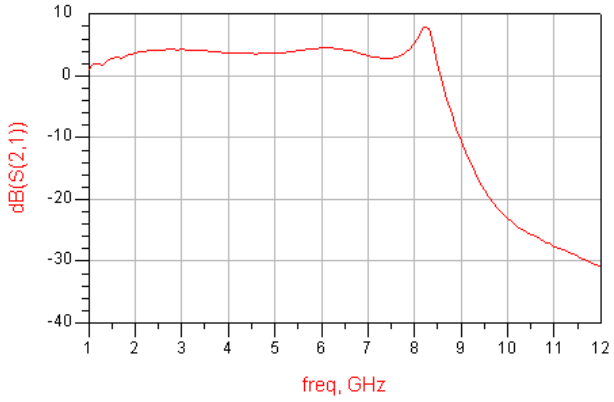

Fig. 5. Measured power gain of the low power CMOS DA.

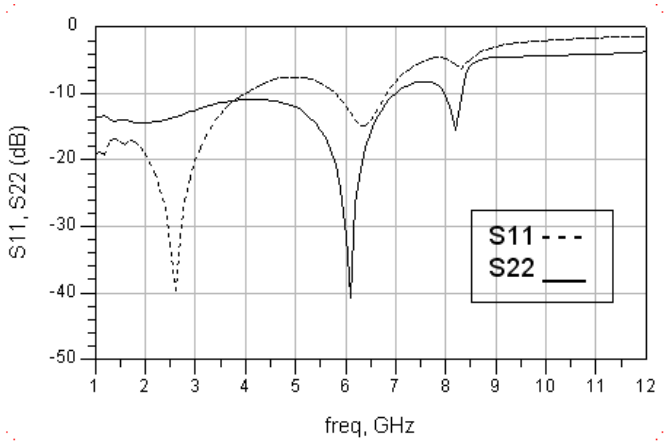

Fig. 6. Measured input and output return loss of the low power CMOS DA.

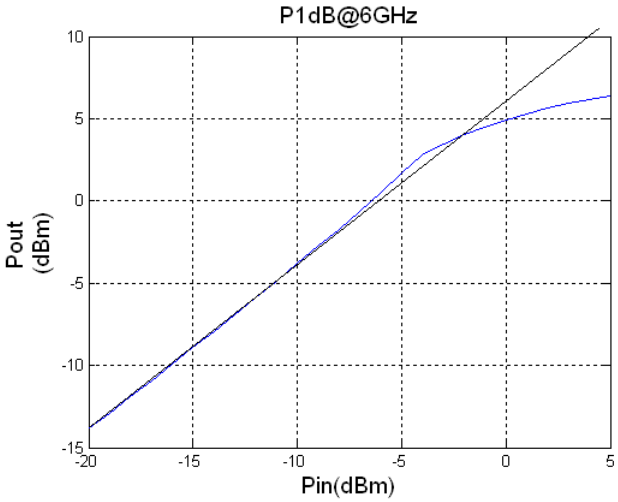

Fig. 7. Measured input referred 1dB compression point of the low power CMOS DA.

Z_d were chosen to be 50Ω. To achieve the goal of low power consumption, the bias current of each amplification stage is fixed to be 4 mA.

IV. Measurement Results

The low power CMOS DA was tested via on-wafer probing. The presented DA has a 8-GHz bandwidth, which covers the frequency range of band groups 1, 2, and 3 of UWB applications, and 4-dB gain with 0.4-dB variation in the band of interest as shown in Fig. 5. Fig. 6 shows the maximum input return loss is -7.6 dB at 5 GHz and the S_{11} is below -10 dB up to 7 GHz. The output return loss has a maximum value of 8.3 dB at 7.7 GHz and below 10 dB up to 8.3 GHz. One-tone test of 6 GHz is performed to measure the input referred 1dB compression point (IP1dB). Fig. 7 shows the meaureded P1dB is 4 dBm. The measured output referred third-order intercept point (OIP3) is 13 dBm by two-tone test with signals of 6 GHz and 6.2 GHz. The measured noise figure of the low power CMOS DA is 4.7-6.1 dB in the frequency band of interest, as shown in Fig. 8. The presented DA only draws 12.9 mA from a 1.8-V supply. The performance is summarized in Table I, with comparisons to other recently published broadband amplifiers.

V. Conclusion

A low power DA has been designed, analyzed, fabricated and measured using a 0.18-μm CMOS technology. The DA employs current reuse technique to lower power consumption and demonstrates a gain of 4±0.4 dB up 8 GHz to cover the frequency range of band groups 1-3 of UWB applications. The power consumption is reduced to be as low as 23 mW. The presented DA provides an approach to meet low power design requirement for UWB applications in the future.

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TABLE I

PERFORMANCE SUMMARY

	Gain_{max}	BW	NF	OIP3	$\text{OP}_1 dB$	Power
this work	5.2 dB	0.01-8 GHz	4.7 dB	13 dBm	4 dBm	23 mW
[8]	11.5 dB	0.01-14 GHz	3.4 dB	20 dBm	10 dBm	52 mW
[9]	8.1 dB	0.01-22 GHz	4.3 dB	16 dBm	5.3 dBm	52 mW
[10]	5.8 dB	DC-6.3 GHz	3.4 dB	N/A	N/A	50 mW

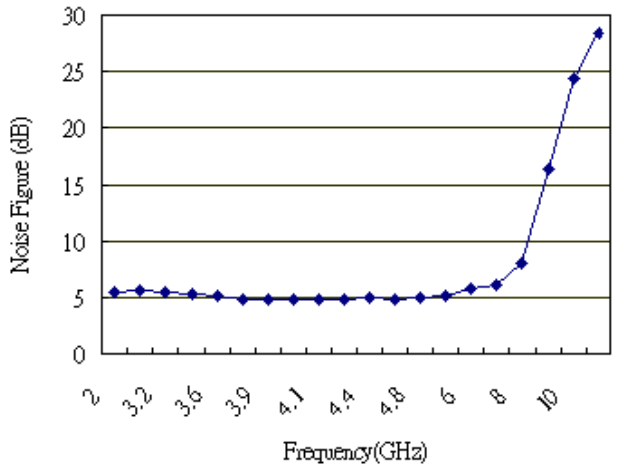

Fig. 8. Measured noise figure of the low power CMOS DA.

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