

A Discrete Fully Logical and Low-cost sub-nanosecond UWB Pulse Generator

Jean Schwoerer⁽¹⁾, Benoit Miscopain⁽¹⁾, Bernard Uguen⁽²⁾, Ghais El-Zein⁽²⁾

⁽¹⁾France Telecom R&D Tech/One - 28 chemin du vieux chênes 38240 Meylan - France
{jean.schwoerer,benoit.miscopain}@francetelecom.com

⁽²⁾IETR-Insa – 20 av des Buttes de Coesmes 35043 Rennes - France
{ghais.el-zein,bernard.uguen}@insa-rennes.fr

Abstract

This article deals about pulse generation for impulse radio applications. The main goal is to realize an FCC-compliant pulser with usual "commercial off-the-shelf" components. The pulser must be easily controlled by the transmitter logic. This is highly desirable for integration in low power equipment with a silicon portable schematic. After a short advantages and drawbacks overview of pulse generation techniques, with their advantages and drawbacks, we describe a solution that properly fits our needs. Several prototypes have been realized and tested. Results of experimentations and measurements are provided and different ways to improve performance and flexibility, in term of power and spectrum management, are also explored.

1. Introduction

An UWB pulser is an RF device needed for many UWB Impulse Radio experiments. In order to fulfill this need, some high-end laboratory pulsers exist on the market and several papers have been published on pulser realizations using Step Recovery Diode (SRD) or avalanche transistor. Herein, the goal is broader: it is not aimed only to realize a laboratory pulser but also to carefully evaluate the feasibility and performances of a future integrated pulser.

In a first step, we roughly present a short overview of different solutions to generate a sharp impulsion and detail the selected solution, with respect to the specified needs.

We then present an implementation of this solution and the associated results. This work is then used as a basis to improve the performances and add flexibility. Results obtained in that respect are also presented.

2. Requirements

The first step is to produce a base-band doublet pulse, and then to shape it in order to keep only the signal energy above 3.1 GHz according to the FCC regulations. This means that before the reshaping, the largest amount of energy of the pulse must be above 3.1 GHz. This means that the pulse duration must be under 500ps. For correct matching with different antennas, the desired output impedance Z_{out} is 50 Ohms and the pulse peak voltage must be at least 500 mV on this 50 Ohms load.

To provide maximum experimentation capability and to reflect real conditions of use the pulser also needs to be easily driven by a standard logic circuitry (it means TTL or LVTTTL pulse trigger), and be able to flawlessly work from very low to very high pulse repetition frequency (PRF).

3. Pulse generation technics

Generating an impulse of a few nanoseconds can be done easily with two logic gates: an inverter and a NAND or XOR gate (see Fig. 1).

In such a "logical pulser", the width of the pulse is defined by the propagation delay T_{pg} in the inverter. But pulse edges mainly depend on the rise time T_r and the fall time T_f of the output stage of the final gate.

The T_{pg} of the inverter can be overcome by adding a short delay line on the other input of the NAND and thus shorten in the deskew between the two edges. But limitations like T_r and T_f are more serious. In fact, these are the true limiting factor of such a pulser, and generally prevent from making any impulsion shorter than one nanosecond.

With standard logic gates, as HCMOS, it is very difficult to get a pulse shorter than 4 ns. However if this simple design is implemented in a high speed FPGA, it becomes possible to obtain a 1 to 2 ns wide impulsion.

Those structures look attractive because :

- They involve no analogue parts, which are difficult to embed in silicon.

- They are easily be controlled by a clock edge.
- They have not any strong limitations as relaxation time between the pulses.

In fact, this kind of structure is a very serious candidate for an silicon realization. But for a discrete components prototype, limited T_r and T_f of classical CMOS or TTL logic gates prevents from getting a sufficiently short pulse.

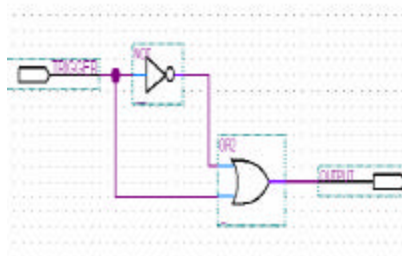


Fig. 1 : Schematic of a logical pulser

Different solutions exist to cross the nanosecond boundary, like using SRD diodes[1,4] which can lead up to a 200 ps pulse but this pulser architecture needs relatively high voltage (compared to the 3.3V of a CMOS) and can not easily be integrated into silicon. In addition, their behavior and thus the way to control it is very different than the one of the "logical pulser"[3]. Such a pulser will be only a lab-tool and not device representative of a future integrated pulser.

4. Ecl logic families

ECL logic is a very high speed silicon bipolar logic family that works in the linear zone rather than in commutation. According to their characteristics, they can provide impulsions of 600 to 700 ps width with 600 mV peak voltage on a 50 Ohms load. As all outputs are differential, an ECL realization will produce both a positive and a negative pulse.

Thus, this logic family seems able to make a pulser whose performances and behavior can be close to the ones achieved by a CMOS implementation.

A first pulser has been built with PECL logic components and as been able to produce the expected impulsions (ie 600 to 700 ps wide and 500 to 600 mV peak). Additionally, it has been able to support PRF up to 100 MHz, and has proved to be easy to control. In

fact the trigger is a TTL rising edge which implies no serious constraints on the control signal.

These first results were encouraging but it was still necessary to improve performances to meet the fixed requirements.

5. Extended performances

The following modifications of the design allow us to improve pulser performances:

- A delay line is added to reduce the deskew between *Trigger* and *Trigger*. In the first design, it was only fixed by T_{pg} , the propagation time in the inverter. This allows a better control of the pulse duration.
- As the pulser is designed to produce a pulse and an inverted-pulse, we can take advantage of these outputs to form a doublet.
- This doublet is produced by introducing a deskew between the pulse and the inverted pulse and recombine them. If this deskew is shorter than the pulse width, it sharpens edges and shortens the doublet duration leading to a better spectrum efficiency at the cost of a power loss.

Concerning the deskew between *Trigger* and *Trigger*, a 6 cm delay line is introduced on the pulser PCB to shorten the pulse right out of the OR gate by 200ps. In order to reduce pulse duration, it would have been possible to shorten more the delay line length but doing so increase dramatically the power loss. Empirically, we stated that the minimum pulse duration is bounded by $T_r + T_f$. Below this limit, peak voltage of the pulse falls very quickly and the pulse bandwidth does not increase anymore.

Generating a doublet instead of a single pulse is very interesting because it suppresses the DC-component and as a consequence increases the pulse power spectral density in the targeted bandwidth.

This doublet will be created by recombining the pulse and the inverted pulse with a delay between them shorter than the pulse width.

An UWB power coupler is required to realize this operation with a good matching and isolations between inputs.

Several well known power coupling structures have been studied.

- A strip-line coupler can be wideband but unfortunately, it is very difficult to achieve a 3db coupling coefficient.

- A Lange coupler as a better coupling coefficient, but causes a lot of ringing. Each pulse is echoed by each open-circuit termination, thus leading to an unacceptable impulse response.
- A hybrid has difficulties to be wideband enough, and has a phasing problem: one input is phase-inverted with the other, thus leading to a destructive recombination.
- A Wilkinson coupler with a ring geometry appears to be wideband enough, with a good isolation and coupling performances. Simulation results are shown in Fig. 2.

Considering results obtained in simulation, it was clear that the Wilkinson coupler is a suited choice, with respect to our needs.

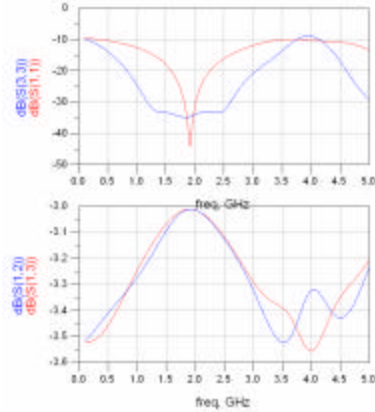


Fig. 2 : Simulation results of the wilkinson

The needed skew between the pulse and the inverted pulse is obtained by adding a short length of strip-line on one of the two inputs. This length was calculated to allow the inverted pulse to start just when the pulse is at its maximum. This trade-off enables to double the slew rate of the descending part of the doublet and contribute to the maximization of pulse energy in the highest part of the band.

6. Realization

This section presents a first realization of this pulser made of ECL logic gates from On-Technology: (see Fig. 3). It relies on two OR gates from an MC100EP01

circuit and a TTL to PECL translator (MC100ELT20). The first OR gate is used as an inverter and the second produces the pulse. Thus, as RF energy is only present on the very short trace between the outputs of this gate and the SMA output connector, the pulser can be realized in standard FR4 Glass Epoxy. The Wilkinson coupler is realized with micro strip-line on Teflon Glass (thickness = 0.8mm and $\epsilon_r = 2.2$).

When correctly optimized, results show a serious increase in performances: The resulting doublet is 500 ps width, shows a center frequency of 1.7 GHz with a -10 dB bandwidth from DC up to 3.7 GHz and presents an output peak to peak voltage of 400mV. Additionally, this pulser was able work up to a pulse repetition frequency of 100 MHz, which is far beyond what can be achieved by a SRD pulser.

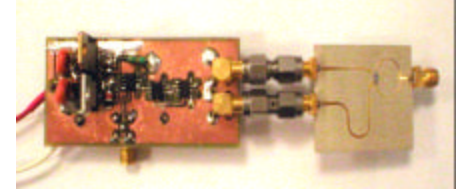


Fig. 3 : ECL pulser with the Wilkinson power combiner

These results are close to the physical component limits: The output stage of the final logic gate is unable to provide the sharpened edges required to increase the upper cutoff frequency.

A new pulser is currently under testing and should provide better performances: it is built on a new generation of ECL logic components based on a SiGe process. Results are not yet available, but according to results of the previous experiences, it should be possible to generate pulse close to the 100ps boundary.

7. Flexibility and pulse shaping

The different circuits described here produce mono-pulse that can be transformed into doublet via recombination of the pulse and the inverted pulse. But more complete pulse shaping capabilities are often required to fit the targeted spectrum constraint. Furthermore, pulse shaping capability is often linked to flexibility requirement in the pulse shape to enable a same pulser to fit different constraints depending on applications and regulatory.

The first solution to fit the signal in the targeted band is to use a band-pass filter. Several tests were

made with commercially available ceramic filters and demonstrated good results: with such a filter, the doublet is turned into a wavelet which is 1.3 ns long and has 1.5 GHz of bandwidth (Fig. 4) from 3.1 to 4.6 GHz. But after filtering, output level is quite lower and an amplifier is required to obtain the targeted 500 mV peak voltage. Different MMIC from Mmicircuit (LEE-39 especially) were tested and give good results with only small distortion of the wavelet.

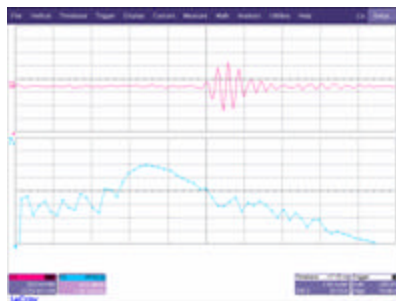


Fig. 4 : Wavelet measured after filtering

The main drawback of this solution is that an important amount of RF energy is lost in the filter. This emphasizes the need to maximize the in-band RF energy before filtering to minimize RF loss.

Another way to shape the pulse is to combine different elementary impulsions in a way that reduces the out-of-band part of the energy.

This kind of recombination gives control on the central frequency, but not the bandwidth, which depends rather on the pulse width. As explained, this width depends on the time difference between arrival of a clock rising (or falling) edges on inputs of the NAND. This deskew can easily be controlled by a delay line inserted in the path of at least one of those signals.

First version of pulser includes a fixed-wire delay line, that is efficient but touchy to set and of course non-modifiable. Software control can be obtained via the use of programmable delay lines. Some of the commercially available logic delay lines give controls of this deskew within 10 ps resolution. This allows easy and accurate control of pulse width and associated spectrum aspect.

Another solution could be the use of variable capacitor (varicap diode, or commuted capacitor) to soften the edges of one of the two clock signals. This would delay the moment when one of the clock signal

cross the threshold between logic 0 and logic 1 levels and give an artificial and controllable delay between the two clocks signal. This solution seems to be simpler at first sight, but due to the cost of a capacitor in CMOS process, this needs further investigations.

8. Conclusion

A very simple pulser structure, built with current off-the-shelf components, for sub-nanosecond pulse generation has been shown with results reaching the requirements. A 500 ps pulse can be obtained with classical logic components and a very limited analog section.

Different solutions are also provided to enhance performances and spectral efficiency. Some of them have been tested, and results have been presented. This leads to present an FCC-compliant pulser, 50 Ohms output impedance, with a very minimal analogue part and very easy to build and to control.

Limitations of this architecture and of the used components are also better understood. Measurements are on-going with more advanced SiGe logic components and should provide, according to previous experimentations, a pulse as short as 100ps.

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