Design and Optimization of a 5 GHz CMOS Power Amplifier

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Abstract— **RF CMOS power amplifier is designed for WLAN 802.11a applications. The fully integrated differential power amplifier, operating in the 5-6 GHz bands, is implemented in a 0.18um IBM 7WL BiCMOS SiGe process using CMOS transistors. This process has seven metal layers and thin-oxide metal-metal capacitors which are high density. As a result, the chip size as well as the cost of the complete power amplifier is reduced. The configuration of the power amplifier is a three-stage cascaded structure with a common source-common gate cascode and a 3.3V supply voltage. The packaged power amplifier with bondwire and package models has a 22.8dBm P1dB compression output power with a 24.1dBm saturation output power, an overall power added efficiency of 22.6%, and a power gain of 30dB in simulation.**

I. Introduction

Power Amplifiers (PA) are the last output stage in a transmitter architecture and determine the overall power efficiency of a transmitter. Power amplifiers are widely used in various wireless transceiver applications including portable communications and Wireless Local Area Network (WLAN) systems. Using microwave technology, WLAN systems transmit and receive data over the air while minimizing the need for wired connections.

As the demand for WLAN IC systems increases, market producers find designing cost efficient circuits is necessary. Traditionally, for designing transmitter chips, GaAs and SiGe processes have been commonly used in the final stage due to their superior device performance. The major design concerns, at present, are achieving a highly integrated system in a single chip, achieving higher yields (with few defects per wafer), and reducing the cost of the chip. The only solution for such goals may be Complementary Metal Oxide Semiconductor (CMOS) technology. Designing in a CMOS process is a popular option in developing wireless transceiver building blocks.

A design with three stages of cascaded amplification is specified to achieve the required gain, more than 25dB. The output stage is designed to provide maximum undistorted output power because it is critical for the PA power performance.

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A differential architecture is chosen for the PA design because of the advantages of reducing the effect of ground inductance as well as canceling the noise and even harmonics. Since a differential PA drives the single-ended input of a system, an extra circuit converting from a differential output to a single-ended input should be designed and placed after power amplifier output (balun or transformer) at the expense of mismatch and efficiency.

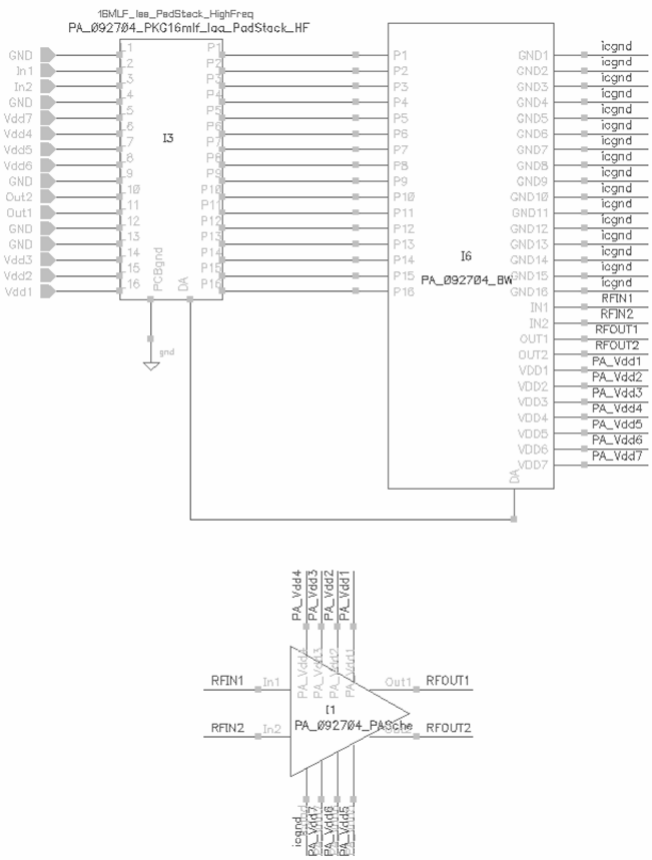


Fig. 1. 5 GHz CMOS Power Amplifier with Bondwire and Package Models.

Figure 1 shows the entire circuit diagram which consists of the PA (on-chip), the bondwire model, and the package model. An example of a CMOS PA in a WLAN transceiver is in [1]. This early example had poor efficiency. This paper presents a

fully integrated 5GHz CMOS power amplifier with on-chip input and output matching networks and good efficiency.

II. CMOS POWER AMPLIFIER CIRCUIT DESIGN

This section describes the CMOS PA design focusing on optimizing the performance. Give the specification of a 5GHz WLAN PA; the complete design process includes device size selection, circuit design, circuit modeling and simulation, and physical layout. The PA has three stages to provide sufficient gain as shown in Figure 2. To achieve the desired output power at the PA output, 10 parallel transistors with a unit transistor size of 100μm width for the output stage are connected together. The amounts of DC currents of each stage on a differential branch are about 5, 20, 100 mA, respectively. The cascode current mirrors with the ratio of 1:5, 1:20, and 1:100 are used in each stage as biasing circuits of the PA. To prevent bias oscillation in the low frequency band, proper bypass capacitors are placed on the paths between power supply and ground and also dc bias and ground.

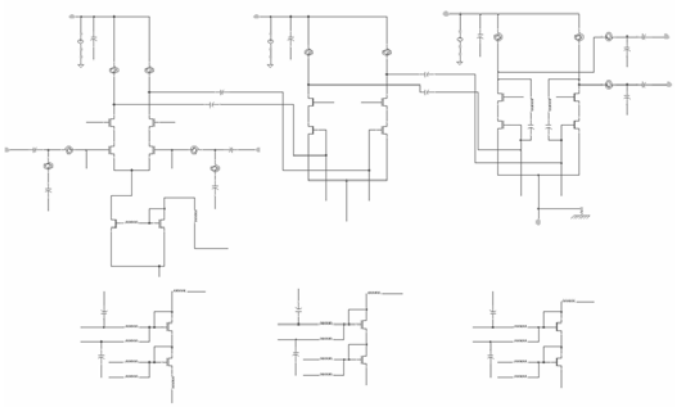


Fig. 2. Complete CMOS Power Amplifier Schematic.

A microphotograph of the fabricated CMOS power amplifier is shown in Figure 3. The chip area is 1.8mm x 1.8mm ($3.24mm^2$) including the 27 bonding pads. In power amplifier applications huge amounts of current flow and electromigration (EM) rules are carefully considered in the layout. Due to the EM failures caused by extremely high current density, metal width which is determined by the amount of current for the bias for each stage was calculated[1]. To minimize the parasitic effects on the drain interconnections of the ten parallel MOSFETs in the output stage of the PA, a special metal structure is used.

Output power, linearity, and power efficiency are the most important parameters in characterizing PAs. In addition, gain, stability, bias network, and matching networks are also important. The PA is the most power consuming part in a transmitter and therefore critical in designing a higher efficiency transmitter. Linearity is also another key design parameter. Existing linear and nonlinear PAs are categorized by circuit configuration, operational topology, biasing point,

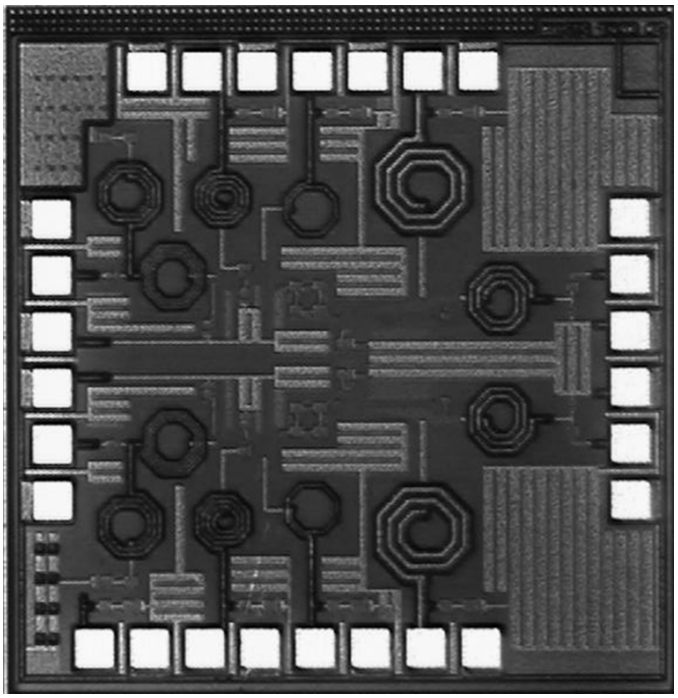


Fig. 3. Die Microphotograph of the CMOS Power Amplifier.

modulation type, linearity, and efficiency [2], [3], Class A PAs which are the most linear are chosen at the cost of efficiency because of its stringent linearity requirement for a WLAN 802.11a application. The design should provide sufficient linearity while maintaining reasonably high efficiency. A tradeoff between the efficiency and linearity is required in PAs. In the practical design of CMOS PAs, efficiency will be decreased by considering the necessary matching network and a finite circuit saturation voltage. Severe reduction in efficiency can occur when packaging the amplifier due to the IC package performance.

Load-pull is necessary to find the optimum load impedance point for the PA to obtain maximum output power while changing the load impedance value on the Smith Chart. Load impedance is chosen with a compromise between PAE and power delivered. Then, an output matching network is designed to set the desired impedances sought from the load-pull test. However, it is not possible to match the entire frequency band of interest. In Figure 4, a single-ended load-pull block diagram is illustrated[2].

The optimum output stage was designed using both a complex conjugate matching method and a load-line and a load-pull approach for the purpose of obtaining maximum power transfer and maximum output power, respectively. The feedback circuit in the output stage is placed between the gate and the drain of cascode transistor to guarantee the stability. Load-pull simulations were performed for each of the three stage outputs to optimize the interstage matching network between stages.

[1] The metal widths are calculated using Table 148 in the IBM 7WL design manual.

[2] This block diagram is captured from RFIC dynamic link in Agilent ADS software.

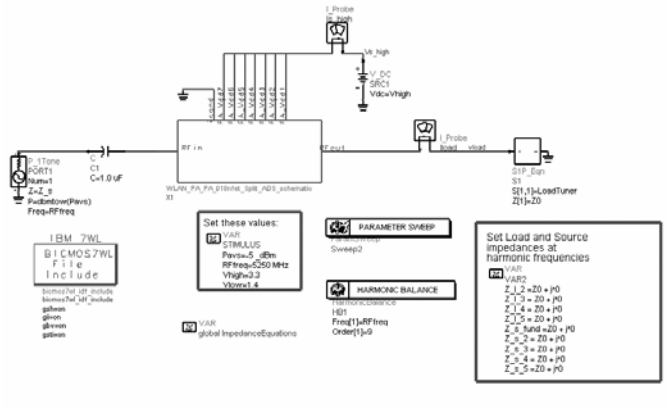


Fig. 4. Load-pull Simulation Block Diagram.

Since the bondwire and package parasites significantly affect the PA performance, the entire PA schematic should take account of both bondwire and package parasitic models during the simulation. The parasitic effects should be considered in the whole design for an accurate correlation between simulation and measurement results. Estimated bondwire and package models in PA design are included in the simulation. Additionally, Micro Lead Frame (MLF) 4 x 4 16-pin package manufactured by Amkor Corporation is used in this research, to house the PA in this work.

III. SIMULATION RESULTS

In this section, the simulation results are presented for the 5 GHz CMOS PA design. Results from various simulations were performed: single-tone, two-tone, S-parameter, and load-pull tests. The test schematic including bondwire and package models for PA simulation is presented in Figure 5.

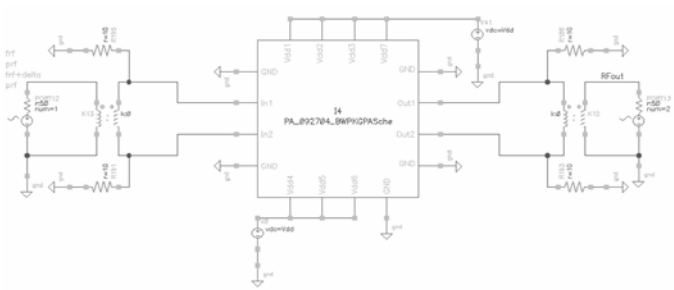
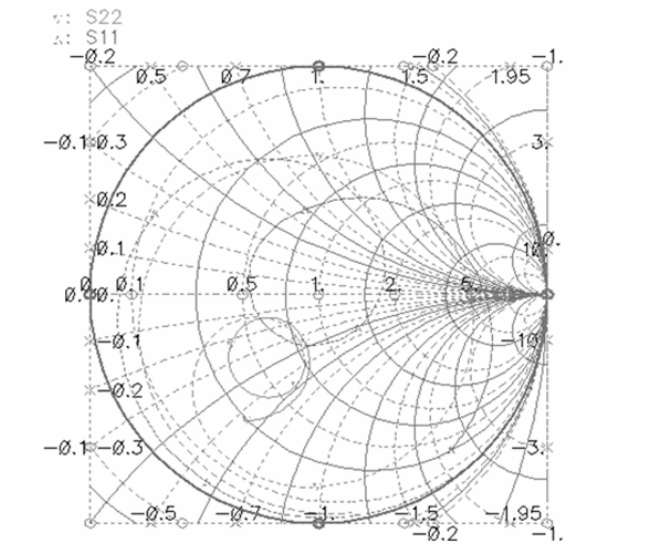


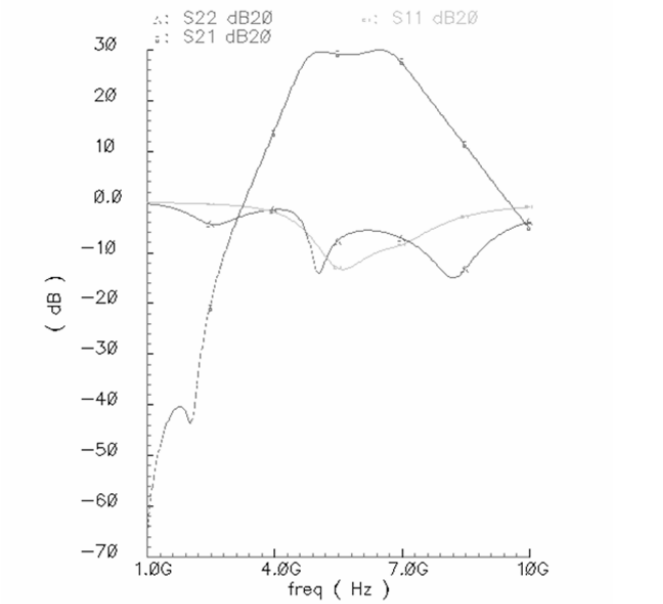
Fig. 5. Power Amplifier Test Circuit for Simulation.

First, the top of Figure 6 shows the PA s-parameter plot which measures the small-signal reflection coefficients S_{11} and S_{22}. Figure 5b shows the s-parameter gain magnitude of the amplifier $|S_{21}|$and input and output isolation on a dB scale. The small-signal gain, $|S_{21}|$ is near 30dB and input and output s-parameters, $|S_{11}|$ and $|S_{22}|$ are less than -10dB in band of interest.

The gain / power compression simulation result from the single-tone test is shown in Figure 7. This figure presents output power, gain, efficiency, and AM-PM conversion along



(a) S_{11} and S_{22} in Smith Chart



(b) Gain and Input / Output Isolations in dB

Fig. 6. S-parameter Plots from 1 to 10GHz.

with input power. Input power is swept from -30dBm to 0dBm with 1dB steps. The output 1dB compression point which can be seen by gain and output power plots is 22.8dBm with 24.1dBm of saturation power. The power added efficiency (PAE) is 22.5% at the P1dB compression point.

A two-tone test is another way to measure PA nonlinearity. A two-tone test with 50MHz spacing (with two fundamental frequencies, 5.25GHz and 5.3GHz) was performed at -15dBm input power which is normally 10dB away from the P1dB compression point. The resulting intermodulation products plot is shown in Figure 8. This two-tone test plot is obtained from the DFT of the large-signal transient simulation up to 150nS. From this plot, the 3rd-order Intermodulation Distortion ratio (IMD3) is 30.5dB and 3rd-order intercept point is 30dBm. In the

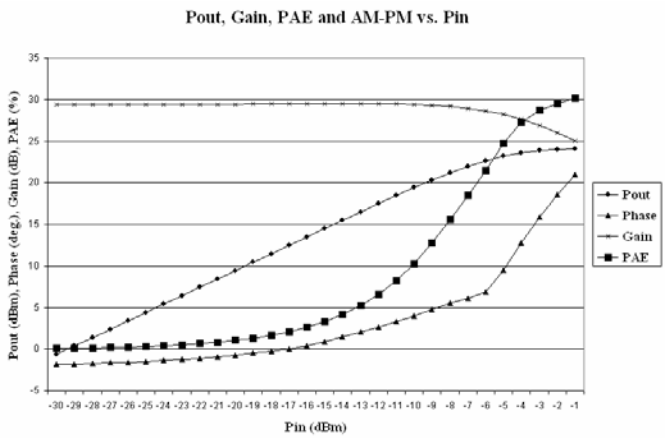


Fig. 7. Gain, Output Power, PAE, and AM-PM vs. Input Power Plot.

future, EVM, ACPR, MTPR, and output spectrum mask test for WLAN 802.11a OFDM signal will be measured.

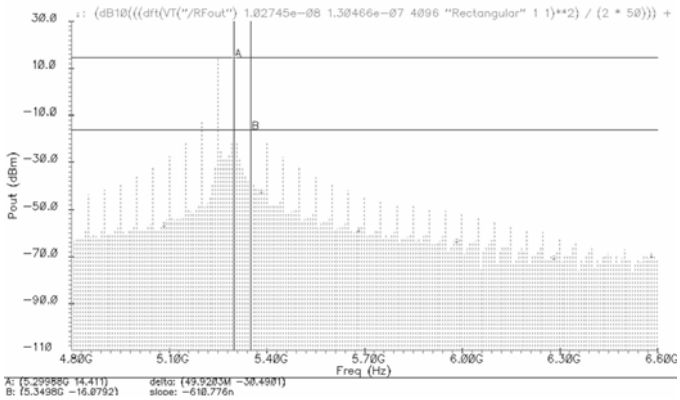


Fig. 8. Intermodulation Products from the Two-Tone Test.

To evaluate the performance of the PA in design, a variety of simulations were performed. Since the bondwire and package parasitic models are included in the simulation, the simulation results are close to the measurement results. Table I summarizes the overall results from the simulation of the CMOS PA.

TABLE I
CMOS POWER AMPLIFIER SIMULATION PERFORMANCE

Parameters	Simulation Results
Frequency Band	5.15 ~ 5.35 and 5.725 ~ 5.825 GHz
Vdd, Id	3.3 V, 256 mA
P1dB	22.8dBm @ Pin = -6dBm
Psat	24.1dBm
Power Gain	29.8dB
Power Efficiency, PAE	22.6%, 22.5%
TOI	30dBm
IMD3	30.5dB @ Pin = -15dBm

Several commercial PAs designed with GaAs and SiGe BJT technologies for 5GHz WLAN applications are measured to compare the performance (Table II). Also Table II shows the results of two published papers and the simulation performances of this research. Evaluating the distortion measurements such as two-tone intermodulation distortion and multi-tone power ratio over the power range in PAs requires a significant amount of data capture and time. Considering the engineering design iterations encountered in IC development, semi-automated Automatic Test Equipment (ATE) set-ups in the engineering lab are used. After setting up the automated test for those commercial PAs, the measurement is expected to be very efficient and accurate [5].

TABLE II
POWER AMPLIFIER COMPARISON TABLE

Power Amplifiers	Gain (dB)	P1dB (dBm)	Idc (mA)	PAE (%)
Company A	15.2	23	244	23
Company B	33.1	22.4	462	11.4
Company C	21.6	15.8	99.3	12.5
Company D	21.6	15.5	163.7	6.5
Paper 1 [4]		22 (Psat)	230	Poor
Paper 2 [5]	15.1	15.4	85	27.1 (Max)
This Research	29.8	22.8	256	22.5

IV. CONCLUSION

In this paper, a fully integrated differential CMOS PA was designed with the 0.18μm IBM BiCMOS 7WL process for a 5GHz WLAN transmitter. The paper also describes a power amplifier design procedure. This CMOS PA provides superior performance in output power, linearity and efficiency compared to those of published papers. This research provides the possibility of CMOS power amplifier with high performance for WLAN applications. In addition, measurement results to date will be presented.

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