Slow-wave Phase Shifter Model and Applications

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ABSTRACT

A true time delay multi-bit MEMS phase shifter topology based on impedance-matched slow-wave CPW sections on a 500μm thick quartz substrate is presented. A semi-lumped model for the unit cell is derived and used in predicting the 4-bit phase shifter performance by cascading N-sections. Experimental data for a 4.6mm long 4-bit device shows a maximum phase error of 5.5° and S_{11} less than -21dB from 1-50GHz. This multi-bit phase shifter is used in an electronically tunable TRL calibration set. It is shown via calibration comparison method that the accuracy of the tunable TRL is close to a conventional multi-line TRL calibration. A maximum error bound of 0.14 at 50GHz is validated using a 0.3pF capacitor on CS-5 substrate and a 100Ω load on GaAs substrate.

I. INTRODUCTION

The DMTL, initially reported by Barker, et al [1], usually consists of a uniform length of high impedance coplanar waveguide (CPW) transmission line that is loaded by periodic placement of discrete MEM capacitors. The increase in the distributed capacitance in the down-state provides a differential phase shift ($\Delta\phi$) with respect to the phase in the upstate. Analog (continuous $\Delta\phi$) versions of the DMTL indicate low-loss performance at *V*- and *W*- band frequencies. However, for reliable operation and to reduce noise in the system a digital design is usually preferred. Assuming a quasi-TEM model for a DMTL unit cell the $\Delta\phi$ is derived as shown in (1) [1]:

$$\Delta\phi = \left(\frac{\omega Z_o \sqrt{\varepsilon_{eff}}}{c}\right) \cdot \left(\frac{1}{Z_u} - \frac{1}{Z_d}\right) \qquad rad \qquad (1)$$

These MEM devices are typically designed such that S_{11} is less than -10dB for the two phase states. Assuming a spacing (s) between MEM capacitors of 200μm and Zo = 95Ω and εr=3.8, Figure 1 shows typical variation of DMTL design parameters; if S_{11}=-20dB is required, the figure shows that the capacitance loading ratio (in the high and low capacitance states) should be 1.05 and the corresponding $\Delta\phi$=168.7° at 50GHz. From this equation, it is clear that for a given unloaded impedance Zo, $\Delta\phi$ increases when the loaded impedances are symmetrically farther away from 50Ω. Furthermore, tight control over the capacitance value is required for S_{11}< -20dB designs, which is one of the limiting factors from a practical standpoint. This

limitation in the capacitively-loaded design restricts the amount of achievable $\Delta\phi$ per unit length in light of impedance matching considerations.
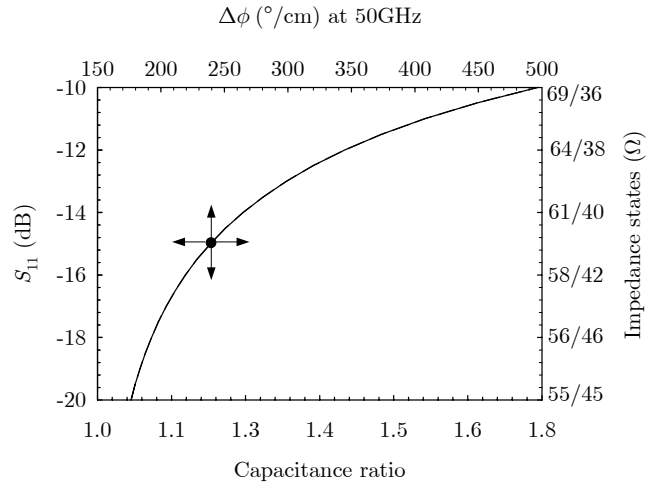

Figure 1: Design curve for a typical DMTL phase shifter design.

In this paper, a new true time delay (TTD) MEM phase shifter based on cascaded slow-wave unit cells is presented that overcomes the limitations of the capacitor-only DMTL. A semi-lumped model for the slow-wave unit cell is derived first and then applied to 4-bit phase shifter by cascading 10 sections (Section II). Experimental results for the multi-bit circuit indicate $S_{11} < $ -20dB and a worst-case $S_{21} < $ -1.3dB. The agreement between measurement and model is within 5%. Using this 4-bit version, an electronic "tunable TRL" calibration set is realized using the 4-bit phase shifter to emulate multiple delay standards in a multi-line TRL calibration. It is shown via measurements that the accuracy of tunable TRL is comparable to a conventional TRL calibration (Section III). The paper concludes with a brief summary.

II. PHASE SHIFTER PERFORMANCE

a. Design and Model for Slow-wave unit cell:

The unit-cell is 460μm long and consists of two beams on each ground plane and a shunt beam that connects the ground planes and is suspended over the center conductor. In the *normal state* the beams on each ground plane are actuated with electrostatic force applied through SiCr bias lines, while the shunt beam is

in the non-actuated state. In this state the signal travels directly from the input to the output. In the *delay state* the beams on the ground plane are in the non-actuated state while the shunt beam is actuated to contact the center conductor. The signal thus travels the longer path through the slot in the ground plane, thereby increasing the time delay. The pull in voltage (V_p) for actuating the ground plane beam and the shunt beam is approximately 35V and 28V respectively. The model for the unit cell in both the states without parasitics is shown in Figure 2.
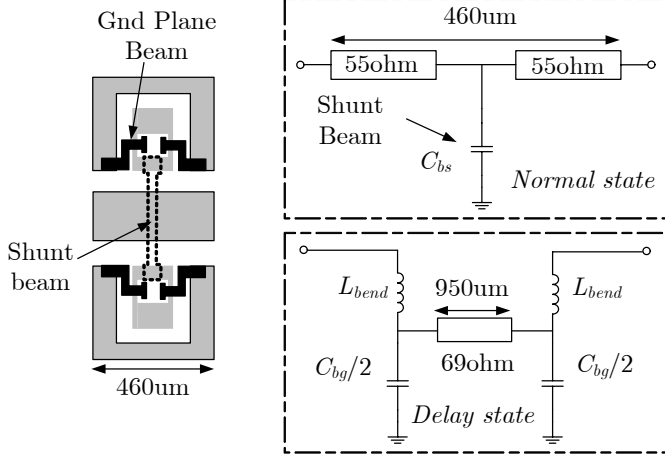

Figure 2: Equivalent circuit model for the unit cell in the *normal* and the *delay state* without parasitics.

The model for a 460μm long slow wave unit cell in the *normal state* is shown in Figure 2. In the *normal state* (Figure 2), the model consists of uniform section of 55Ω transmission line (S/W/S=35/250/35μm) that is 210μm long on each side of the shunt beam. The shunt beam, which is 40μm wide and suspended 1.8-2μm above the center conductor provides a capacitance (C_{bs}) of approximately 8fF (using the parallel plate approximation). Using the per unit length value for line parameters (Capacitance=C_{tn}, Inductance=L_{tn}) and a spacing s=460μm for a 55Ω transmission line, the effective normal state impedance (Z_n) is found to be approximately 50.5Ω using (2) [1]. The effect of bridge inductance is excluded in (2).

$$Z_n = \sqrt{\frac{L_{tn}}{C_{tn} + \frac{C_{bs}}{s}}} \quad ; \quad Z_s = \sqrt{\frac{L_{ts}}{C_{ts} + \frac{C_{bg}}{s_1}}} \quad (2)$$

The total length of the CPW line that is routed through the slot is approximately 950μm. Since the signal is routed through the long slot section, the current bending at the junction is modeled using an inductor L_{bend} and the value is found via circuit optimization. The non-actuated ground-plane bridges provide a total capacitance (C_{bg}) of 2×24fF. A good impedance match in the slow-wave state is made possible by designing the slow-wave section to emulate a 69Ω uniform CPW line The effective impedance (Z_s) for the unit cell is calculated from (2) and found to be approximately 49.54Ω.

The unit cell is fabricated on 500μm thick quartz substrate (ε_r =3.8) and the details of fabrication is presented in [5]. Measurements were performed from 1−50GHz using a Wiltron 360B vector network analyzer and 150μm pitch GGB microwave probes.

b. 4-bit Phase Shifter Performance
Figure 3 shows the schematic of the fabricated 4-bit phase shifter. The multi bit version is designed to provide Δϕ of 45°, 90°, 180° and 225° at 30GHz. The 4-bit version also consists of 10 cascaded slow-wave unit cells (or 5 unit-cell pair). Each unit cell pair provides a Δϕ=45° at 30GHz. For example, in the first bit (Δϕ=45°), only one unit cell pair is operated in slow-wave state while the other pairs remain in the normal state. The second bit (Δϕ=90°), consists of two unit cell pairs operated in the slow-wave state. The transition from the 1st bit to the 2nd bit is achieved by shorting the unit cell pair using a wire-bond between the DC pads. Since the unit cell pairs are identical, there are five non-trivial phase states. Figure 4 shows a comparison between measured and modeled S_{11} and S_{21} data for the 1st bit and the 4th bit. The simulated results were obtained by cascading the equivalent circuit model for the unit cell in the ADS circuit simulator. In this simulation, the beam is modeled as series RLC and these values are found from optimization. For the dimensions used herein, the inductance of the beam is typically between 10-30pH (found via EM simulation). It is seen from these plots that the agreement between measurements and model is good through 50GHz with S_{11} less than -21dB and worst-case S_{21} greater than -1.39dB. It was found via measurement that S_{21} was ~0.45dB greater than that of a uniform 50Ω line of the same length. The additional loss is predominantly due to the contact resistance, conductor roughness and signal leakage via SiCr bias lines.
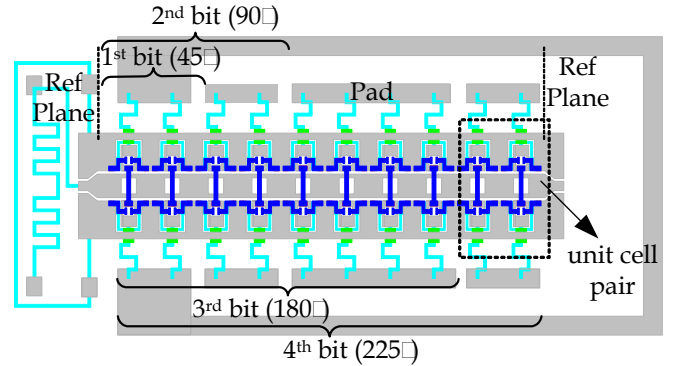

Figure 3: Schematic of the 4-bit phase shifter.

The comparison of Δϕ between measured and modeled data is shown in Figure 5. The agreement between measured and modeled data is good with phase error less than 5.5° at 30GHz.
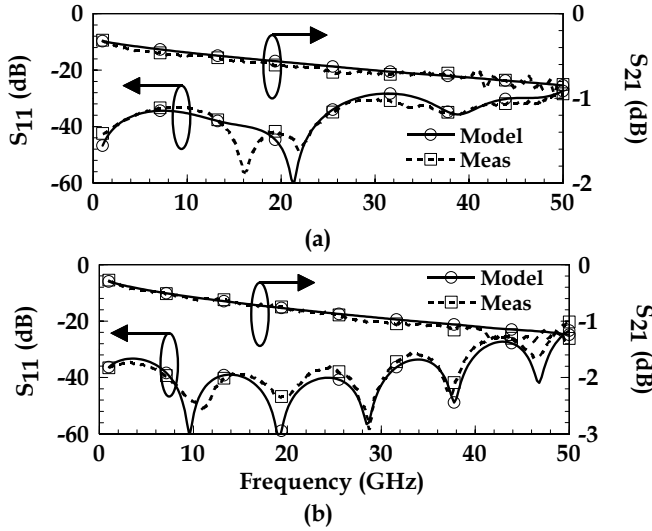
Figure 4: Comparison of S_{11} (dB) and S_{21} (dB) between measured data and equivalent circuit model for the 1st bit (45°) and the 4th bit (225°).
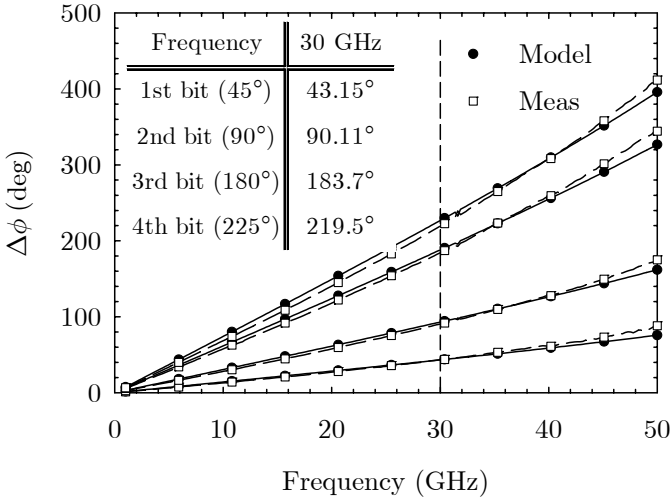

Figure 5: of $\Delta\phi$ between measured and modeled data for the multi bit phase shifter.

III. TUNABLE MULTI-LINE TRL

The MEMS tunable 4-bit phase shifter presented herein is used to realize four delay line calibration standards in a multi-line TRL. The normal-mode operation (or $\Delta\phi=0°$) of the phase shifter mimics the thru standard. The different bits of the slow-wave phase shifter are actuated in order to emulate the delay line standards. The open standard is realized using a separate, uniform CPW line. The effective offset lengths of the delay lines extracted from measured $\Delta\phi$ at 35GHz are approximately 739μm ($\Delta\phi=47°$), 1460μm ($\Delta\phi=93°$), 2931μm ($\Delta\phi=188°$) and 3669μm ($\Delta\phi=235°$).

The results of a Tunable TRL calibration are compared with a calibration performed using uniform CPW line standards on the

quartz substrate. The reference planes for both calibrations are established at the probe tips with Z_0 corrected to 50Ω. Furthermore, same number of line standards was used in both the calibrations. The maximum error bound $|S_{ij}-S_{ij}'|_{max}$ between multi-line TRL standard on quartz (TRL1) and Tunable-TRL on quartz is computed using the calibration comparison method [6]. The comparison was also made between standard TRL on a CS-5[1] substrate (TRL2) and the Tunable TRL, as illustrated in Figure 6.

The calibration comparison method is based on the assumption that a perfect multi-line TRL calibration using conventional standards calculates the true scattering parameters S_{ij} of a device from uncorrected measurement data. However, an imperfect TRL calibration based on standards with errors (Tunable TRL) will result in calibration coefficients which differ from those of the perfect calibration. These imperfect calibration coefficients calculate scattering parameters S_{ij}', which differ from the actual scattering parameters S_{ij}. The calibration-comparison method determines an upper bound for $|S_{ij}-S_{ij}'|$ from differences in the perfect and imperfect calibration coefficients when $|S_{ii}| < 1$ and $|S_{12} S_{21}| < 1$. The upper bounds indicate the maximum possible difference in any of the four S-parameters for a 2-port passive device.
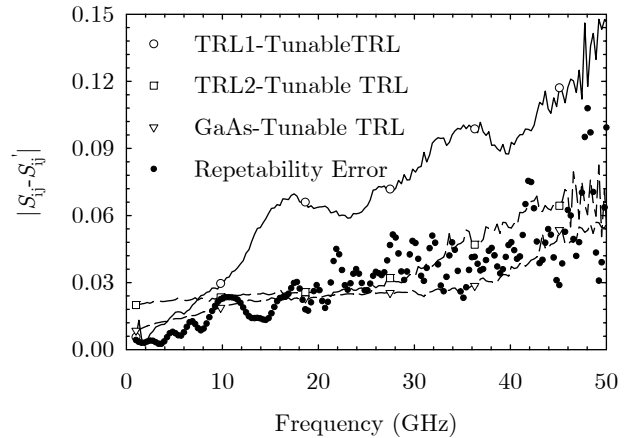

Figure 6: Upper bound error $|S_{ij}-S_{ij}'|_{max}$ between standard TRL and Tunable TRL.

It is seen from Figure 6 that the upper bound between TRL1-Tunable TRL and TRL2-Tunable TRL increases linearly with a maximum bound of 0.14 at 50GHz for TRL1-Tunable TRL calibration sets. The increase in the error bound is due to the slight increase in the insertion loss and a 2% deviation from 50Ω for the 4-bit phase shifter when compared to uniform CPW line. For completeness, the repeatability of the two Multi-line TRL calibrations on the quartz substrate is also shown in the figure.

Verification

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[1] CS-5 is a commercial calibration substrate manufactured by GGB Industries, Naples, FL.

3

A 0.3pF capacitor fabricated on 100μm GaAs substrate is measured after performing a TRL calibration and a Tunable TRL. It is seen in Figure 7a that the measurement results performed using the Tunable TRL and TRL performed on a GaAs substrate agree well. Furthermore, the maximum vector difference between the two measured S-parameters is within the estimated error bounds.

A 100Ω load verification structure was measured on a 700μm thick CS-5 substrate (ε_r=9.9, tanδ=0.002) after performing an on-wafer calibration (TRL2) using uniform CPW line standards. It is seen from Figure 7 (b) that the measurement results performed using Tunable TRL and TRL2 agree well.
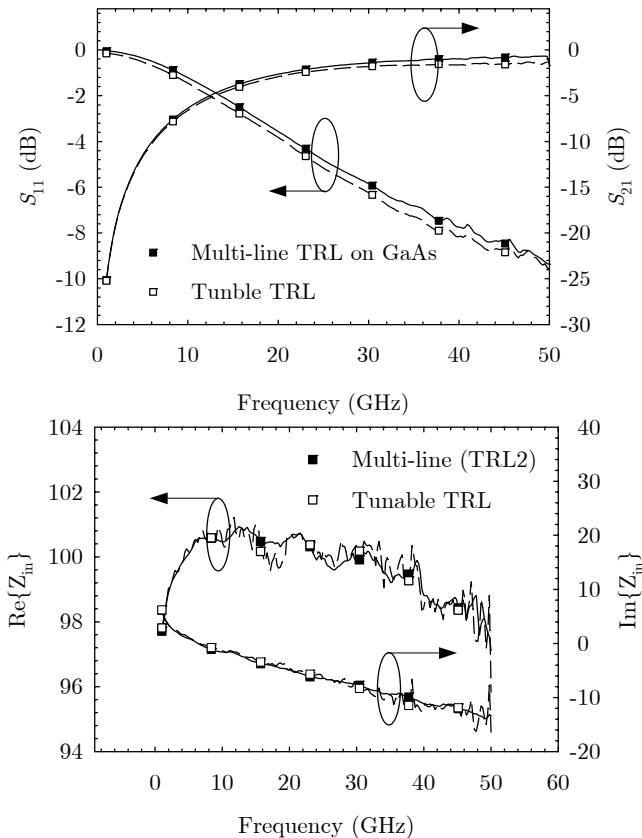

Figure 7: (a) S_{11} and S_{21} of 0.3pF verification structure. The line was measured after a Tunable TRL calibration and a standard TRL on GaAs; (b) Z_{in} (Real and Imaginary) of a 100Ω load verification structure on a 700μm thick CS-5 substrate.

IV. SUMMARY

In this paper, a true-time-delay CPW phase shifter operating from 1-50GHz on a 500μm thick quartz substrate is presented that utilizes slow-wave MEMS sections. A semi-lumped model for the unit cell is derived and shows good agreement with the 4-bit phase shifter measured results. The measured Δϕ for the 4-bit version agree within 5% (~ 5.6° phase error at 50GHz) of the predicted value with worst-case S_{21} less than -1.4dB at 50GHz.

An electronically tunable calibration is made possible by realizing all the line standards using the multi-bit phase shifter in a typical multi-line TRL. The calibration comparison method shows a maximum bound of 0.14 at 50GHz between a Tunable TRL calibration and a standard multi-line TRL on two different substrates. The Tunable TRL method provides for an efficient usage of wafer area while retaining the accuracy associated with the TRL technique, and reduces the number of probe placements from five to two (with potentially no change in probe separation distance).

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